Cost-Effective Compensation Design for Output Customization and Efficiency Optimization in Series/Series-Parallel Inductive Power Transfer Converter

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***Abstract*—Load-independent output with zero-phase-angle (ZPA) input is desirable in wireless inductive power transfer (IPT) converters for effective power delivery, but it usually greatly relies on the parameters of the loosely coupled transformer, normally fixed or constrained by space. Thus, customizable outputs cannot be readily achieved unless a new transformer is redesigned. In this article, we elaborate the rather complex relationships among compensation parameters, customizable load-independent-voltage (LIV) outputs with ZPA input, power efficiency, and overall compensation capacitance cost of the series/series-parallel (S/SP) IPT converter. We present a cost-effective compensation design to free the customization of LIV outputs from a parameter-constrained loosely coupled transformer, with optimization between efficiency enhancement and overall compensation capacitance cost. We conducted the proposed design supported by experimental results in S/SP IPT converters with an identical loosely coupled transformer and various sets of compensation capacitors. Compared with a conventional design, the proposed design provides custom ranges of LIV outputs in both a weak and a relatively strong coupling condition, with over 5.9% and 5% efficiency improvement, respectively. The overall compensation capacitance can also be reduced by up to 37% and 21.5%, respectively.**

***Index Terms*—Efficiency optimization, inductive power transfer (IPT), output customization, series/series-parallel (S/SP) compensation, zero phase angle (ZPA).**

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I. Introduction

DEVELOPMENT in modern power electronics has enabled wireless inductive power transfer (IPT). Benefiting from eliminating physical contact, IPT converters can provide user-friendly and maintenance-free operations of wireless power supply in many applications, such as consumer electronics, electric vehicles, bioimplants, underwater vehicles, and so on [1]–[6]. Voltage buses are widely needed in these power electronics applications and, thus, IPT converters with load-independent voltage (LIV) output are widely studied [7]–[11].

Effective power transfer is a critical demand in most IPT application scenarios, where compensation using reactive components for a loosely coupled transformer [12] is usually designed to achieve load-independent output and zero-phase-angle (ZPA) input, thus eliminating the output control [13], [14] and minimizing the voltage-ampere (VA) rating [15], [16], respectively. Moreover, multiple selectable outputs are desired to meet specific requirements in some application scenarios, where the parameters of the loosely coupled transformer are usually fixed or constrained by space, leading to difficulty in output design [17]. As an example, bus voltage on vehicle side may differ in level depending on specifications of the batteries or supercapacitors, but standard SAE J2954 has suggested a coil and winding geometry specification for wireless electric vehicle charging [18], posing challenges to achieving customizable outputs without redesigning the transformer. Therefore, as a general technical problem in regardless of application scenarios, it is worth optimizing the compensation design for customizable outputs against the constraints of transformer parameters.

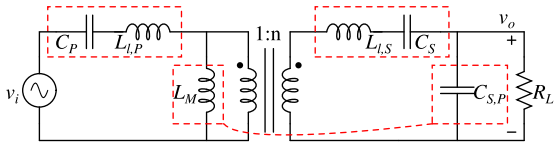


Fig. 1. Conventional design concept of the S/SP IPT converter.

From the perspective of minimizing loss and cost, basic compensation topologies are usually adopted, because they only contain minimum number of external capacitive components, i.e., two capacitors, one at each side of the transformer windings, of which the losses are usually negligible. External inductive components, i.e., inductors, with significant copper and core losses are not needed [19]. Four basic compensation topologies are normally identified according to the primary/secondary compensation type, namely series/series (SS), series/parallel (SP), parallel/series, and parallel/parallel. In [15], design for ZPA input to minimize VA rating is studied covering four basic compensation topologies, but output controllability cannot be achieved. In [13] and [14], characteristics of LIV or load-independent-current (LIC) output as well as maximum efficiency are comparatively studied for the SS and the SP IPT converter. Nevertheless, output to input transfer functions of the SS and the SP IPT converter greatly rely on transformer parameters, e.g., the LIC transfer function of the SS IPT converter and the LIV transfer function of the SP IPT converter are typically $\frac{i_o}{v_i} \approx \frac{1}{\omega k\sqrt{L_P L_S}}$ and $\frac{v_o}{v_i} \approx \frac{1}{k}\sqrt{\frac{L_S}{L_P}}$, respectively [13], [14], which are dependent on the primary self-inductance L_P, the secondary self-inductance L_S, and the coupling coefficient k of the transformer. Once the transformer is designed, the converter transfer functions are almost fixed unless a new transformer is used. Therefore, basic compensation may not provide the required current or voltage output in a particular application scenario.

To overcome the constraints imposed by the transformer parameters, higher-order compensation topologies with more reactive components, usually including inductors, can be used to achieve more design freedom for output transfer functions without altering the design of the transformer, such as LC/LC compensation [20] and LCC/LCC compensation [21]. By changing the compensation parameters, customizable LIV or/and LIC transfer functions with ZPA input can be achieved for a wide range of load. Comprehensively, a family of higher-order compensation circuits for IPT converters are proposed in [17]. With these proposed compensation circuits, LIV and LIC outputs can be easily customized by adjusting the compensation parameters, while ZPA input can always be guaranteed to ensure minimum VA rating. However, the efficiency usually suffers from using inductors with significant copper and core losses, which is a major concern of these higher-order compensated IPT converters [19]. Moreover, relationship between compensation parameter design and efficiency performance has rarely been studied.

As a tradeoff between basic compensation and higher-order compensation, SS/SP (S/SP) compensation without lossy inductors is readily derived for the loosely coupled transformer to easily implement LIV output and ZPA input [7]–[9], with

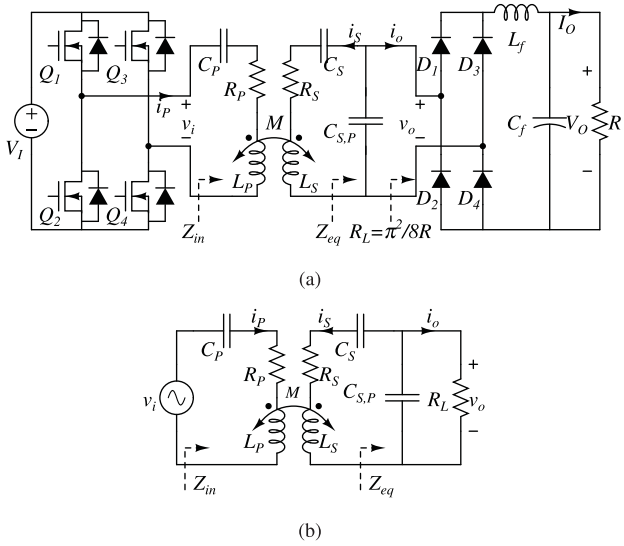


Fig. 2. (a) Schematics and (b) equivalent circuit model of the S/SP IPT converter.

an intuitive design concept illustrated in Fig. 1. The primary leakage inductance $L_{l,P}$, secondary leakage inductance $L_{l,S}$, and mutual inductance L_M of the T-circuit model of the loosely coupled transformer are fully compensated by the external capacitors C_P, C_S, and $C_{S,P}$, respectively, such that the S/SP IPT converter can behave as an ideal transformer with a turn ratio of $\frac{1}{n}$ to achieve LIV output, as well as ZPA input due to pure resistive input impedance. This intuitive design concept fixes the LIV transfer function at a k-independent point featuring misalignment-tolerance, but it does not meet the desired requirement of output customization. Moreover, efficiency performance and overall compensation capacitance cost related to compensation parameters are even more worth being further studied to facilitate the design of the S/SP IPT converter.

In this article, a cost-effective compensation design is elaborated to achieve customizable LIV outputs with ZPA input and optimized power efficiency for the S/SP IPT converter. This article is organized as follows. In Section II, compensation parameters are indicated by a single design factor μ and analyzed to generalize conditions allowing any designs for S/SP IPT converters with an identical loosely coupled transformer to achieve customizable LIV transfer functions with ZPA input. Section III gives criteria for theoretical optimum efficiency, with which the relationship of efficiency improvement and design of μ is revealed, and a critical minimum design value of μ is derived to ensure load matching for optimized efficiency. Section IV optimizes the custom range of LIV outputs between the efficiency performance and the overall compensation capacitance cost, and puts forward a cost-effective design. The proposed design is experimentally verified in Section V. Finally, Section VI concludes this article.

II. Analysis of LIV Output With ZPA Input

Fig. 2(a) shows the schematics of an S/SP IPT converter consisting of an input voltage source V_I, a full bridge inverter, a resonant tank with S/SP compensation, and a rectifier with LC filter.

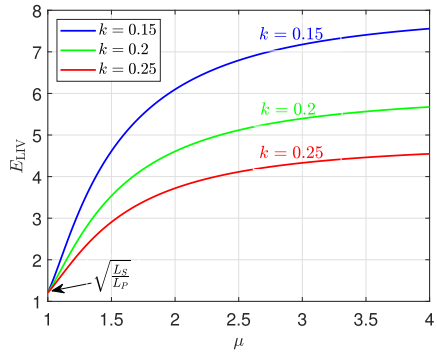


Fig. 3. LIV transfer function $E_{\rm LIV}$ versus compensation design indicator μ.

To generalize the analysis of the input and output of the S/SP IPT converter, Fig. 2(b) shows a commonly used coupled-circuit model based on fundamental approximation [13], [14], where the loosely coupled transformer has primary self-inductance L_P, secondary self-inductance L_S, and mutual inductance M. The coupling coefficient is given by $k = \frac{M}{\sqrt{L_P L_S}}$. C_P and C_S are the series compensation capacitors in each side, while $C_{S,P}$ is the parallel compensation capacitor in the secondary side. Coil losses in the primary and the secondary sides are represented by resistors R_P and R_S. v_i, v_o, and R_L are the equivalent input voltage, output voltage, and load resistor, respectively. Similar to that of the SS IPT converter, C_P and C_S resonate with L_P and L_S at angular frequencies

$$\omega_P = \frac{1}{\sqrt{L_P C_P}}, \text{ and} \tag{1}$$

$$\omega_S = \frac{1}{\sqrt{L_S C_S}} \tag{2}$$

respectively. Their ratio is defined as an indicator of compensation parameter design and given by

$$\mu = \frac{\omega_P}{\omega_S}. \tag{3}$$

In this article, the single factor μ will be investigated to indicate a cost-effective design of compensation parameters, including C_P, C_S, and $C_{S,P}$ of the S/SP IPT converter, for customizing LIV outputs with ZPA input, and optimizing between power efficiency and overall compensation capacitance cost.

A. Customizable LIV Outputs

The coupled circuit equations for the S/SP IPT converter in Fig. 2(b) are

$$\begin{aligned}&(R_P + jX_P)i_P - jX_M i_S = v_i\\ &-(R_S + jX_S + Z_{eq})i_S + jX_M i_P = 0\end{aligned} \tag{4}$$

where $X_P = \omega L_P - \frac{1}{\omega C_P}$, $X_S = \omega L_S - \frac{1}{\omega C_S}$, $X_M = \omega M$, and $Z_{\rm eq} = \frac{1}{j\omega C_{S,P} + \frac{1}{R_L}}$ are the impedance of corresponding components for calculation.

The ratio of the output voltage v_o to the input voltage v_i is defined as voltage transfer function E, of which the calculation is highlighted as

$$E = \frac{v_o}{v_i} = \frac{jX_M}{jX_P + \frac{X_M^2 - X_P X_S}{Z_{\rm eq}}}. \tag{5}$$

Although R_P and R_S are nonzero for a practical IPT converter, it is valid to simplify subsequent analyses of voltage transfer function and input phase angle by assuming $R_P = 0$ and $R_S = 0$ [13], [14], [17]. From (5), the condition to achieve LIV transfer function is obviously given by

$$\omega^2 M^2 - X_P X_S = 0. \tag{6}$$

By solving (6), the LIV transfer function $E_{\rm LIV}$ and the corresponding operating frequency ω_H are given by

$$E_{\rm LIV} = \sqrt{\frac{L_S}{L_P}}\frac{k(\mu^2 + 1 + \Delta)}{(2\,k^2 - 1)\mu^2 + 1 + \Delta}, \text{ and} \tag{7}$$

$$\begin{aligned}\omega_H &= \omega_S\sqrt{\frac{\mu^2 + 1 + \Delta}{2(1 - k^2)}}\\ &\approx \frac{\mu}{\sqrt{1 - k^2}}\omega_S, \text{ for } (\mu^2 - 1)^2 \gg 4\,k^2\mu^2\end{aligned} \tag{8}$$

respectively, where $\Delta = \sqrt{(\mu^2 - 1)^2 + 4\,k^2\mu^2}$. It should be pointed out that the S/SP IPT converter can also achieve another LIV transfer function $E_{\rm LIV}|_{\omega_L} = \sqrt{\frac{L_S}{L_P}}\frac{k(\mu^2 + 1 - \Delta)}{(2\,k^2 - 1)\mu^2 + 1 + \Delta}$ at operating frequency $\omega_L = \omega_S\sqrt{\frac{\mu^2 + 1 - \Delta}{2(1 - k^2)}}$. Similar to the case of S/S IPT converter, operating at ω_H is usually preferred because of better efficiency performance and, thus, chosen for subsequent analyses in this article [7], [8]. From (7), $E_{\rm LIV}$ is customizable with different designs of μ by altering C_P, C_S, and $C_{S,P}$. Fig. 3 shows the customizable $E_{\rm LIV}$ versus μ under different values of k with the simulation parameters given in Table I, which will be used for the rest of this article unless specified. It can also be observed that, $E_{\rm LIV}$ is k-dependent for most designs of μ except the unity design, i.e., $\mu = 1$.

TABLE I
SIMULATION PARAMETERS OF THE S/SP IPT CONVERTER

Parameters	Symbols	Values
Self inductance	L_P, L_S	118 μH, 172 μH
Coupling coefficient	k	0.15–0.25
Coil resistance	R_P, R_S	0.5 Ω, 0.72 Ω
Operating frequency	$\frac{\omega_H}{2\pi}$	50 kHz

B. ZPA Input

ZPA input is important for the IPT converters to minimize VA rating and improve power transfer capability. The input impedance of the S/SP IPT converter shown in Fig. 2(b) is given by

$$Z_{\rm in} = jX_P + \frac{\omega^2\,M^2}{jX_S + Z_{\rm eq}}. \tag{9}$$

To achieve ZPA input, $Z_{\rm in}$ should be purely resistive, i.e.,

$$\Re(Z_{\rm in}) = Z_{\rm in} \tag{10}$$

for arbitrary load conditions. Substituting (8) into (9) and solving (10), design of $C_{S,P}$ for ZPA input can be derived as

$$C_{S,P} = \frac{C_S}{\frac{\omega_H^2}{\omega_S^2} - 1} \tag{11}$$

which is determined by the design of μ.

C. Revisiting of Conventional Design for Misalignment-tolerance

Specifically, for the S/SP IPT converters based on conventional design concept [7]–[9], μ is actually set at unity by properly choosing C_P and C_S to satisfy $\omega_P = \omega_S$. Such that, the LIV transfer function has no relationship with k as given by

$$E_{\text{LIV}}|_{\mu=1} = \sqrt{\frac{L_S}{L_P}}, \text{ at} \tag{12}$$

$$\omega_H|_{\mu=1} = \frac{\omega_S}{\sqrt{1-k}}, \text{ when } \mu = \frac{\omega_P}{\omega_S} = 1. \tag{13}$$

Since the LIV transfer function $E_{\text{LIV}}|_{\mu=1}$ in (12) is k-independent, it is commonly believed that the S/SP IPT converter with such design is misalignment-tolerant and suitable for dynamic IPT applications with k-variation [7]–[9]. However, since the operating frequency $\omega_H|_{\mu=1}$ in (13) is k-dependent, phase-lock loop control is usually needed for frequency tracking against the variation of k [10], [11]. Moreover, $C_{S,P}$ is k-dependent from (11), and additional adaptive control for $C_{S,P}$ is inevitably required to maintain ZPA input against k-variation [22], [23]. Therefore, in practice, it takes a lot of control effort for the S/SP IPT converter to maintain LIV output and ZPA input in dynamic applications [10], [11], [22], [23]. This concern facilitates our implementation of the S/SP IPT converter toward stationary IPT applications with invariable k.

III. Efficiency Optimization

A. Criteria for Maximizing Power Efficiency

Fig. 4(a) gives an equivalent circuit of Fig. 2(b) for analysis of the power efficiency. Z_r is the reflected impedance from the secondary to the primary given by $Z_r = \frac{\omega^2 M^2}{jX_S + Z_{\text{eq}}}$. As usual, by separately considering the efficiency η_P in the primary and the efficiency η_S in the secondary sides, overall power efficiency η of the S/SP IPT converter can be calculated as

$$\eta = \eta_P \eta_S = \frac{\Re(Z_r)}{R_P + \Re(Z_r)} \frac{\Re(Z_{\text{eq}})}{R_S + \Re(Z_{\text{eq}})} \tag{14}$$

where $\Re$ represents calculation of real component.

To analyze the power efficiency in a more intuitive way, the equivalent impedance Z_{eq} is transformed into a form of series connection as shown in Fig. 4(b) and rewritten as

$$Z_{\text{eq}} = jX_{S,P} + j\Delta X_{L,\text{eq}} + R_{L,\text{eq}} \tag{15}$$

where

$$R_{L,\text{eq}} = \frac{R_L}{Q^2 + 1} \tag{16}$$

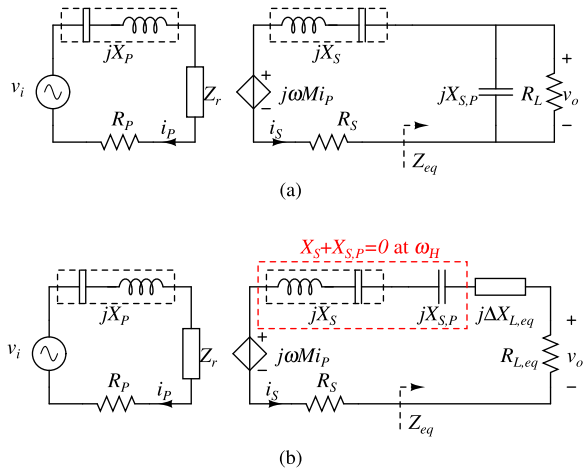


Fig. 4. (a) Equivalent circuit model of Fig. 2(b) with reflected impedance Z_r, and (b) transformation of load impedance in Fig. 4(a) into a form of series connection.

$$\Delta X_{L,\text{eq}} = \frac{R_{L,\text{eq}}}{Q}, \text{ and} \tag{17}$$

$$Q = \omega C_{S,P} R_L \tag{18}$$

are defined as equivalent load resistance, equivalent load reactance, and load quality factor, respectively. Since the S/SP IPT converter desirably achieves LIV output at ω_H, it can be observed that

$$X_S + X_{S,P} = 0, \text{ at } \omega_H. \tag{19}$$

With (14), (15), and (19), the power efficiency at ω_H can be calculated and further simplified as

$$\begin{aligned}\eta &= \frac{1}{\frac{\Delta X_{L,\text{eq}}^2}{R_{L,\text{eq}}} + \frac{(R_{L,\text{eq}}+R_S)^2}{R_{L,\text{eq}}}} \frac{R_P}{\omega_H^2 M^2} + \frac{R_S}{R_{L,\text{eq}}} + 1 \\ &\approx \frac{1}{\frac{\Delta X_{L,\text{eq}}^2}{R_{L,\text{eq}}} + R_{L,\text{eq}}} \frac{R_P}{\omega_H^2 M^2} + \frac{R_S}{R_{L,\text{eq}}} + 1\end{aligned} \tag{20}$$

with the assumptions $\frac{\omega_H^2 M^2}{R_P R_S} \gg 0$ and $R_{L,\text{eq}} \gg R_S$. The optimum values of $R_{L,\text{eq}}$ and $\Delta X_{L,\text{eq}}$ will be found to maximize η. From (20), the efficiency can be maximized as

$$\eta_{\text{opt}} \approx \frac{1}{\frac{2}{k\sqrt{Q_P Q_S}} + 1}, \text{ if} \tag{21}$$

$$R_{L,\text{eq,opt}} = \omega_H M \sqrt{\frac{R_S}{R_P}}, \text{ and} \tag{22}$$

$$\frac{\Delta X_{L,\text{eq}}^2}{R_{L,\text{eq}}} = \frac{R_{L,\text{eq}}}{Q^2} \to 0 \tag{23}$$

where $Q_P = \frac{\omega_H L_P}{R_P}$ and $Q_S = \frac{\omega_H L_S}{R_S}$ are the quality factors of the primary and secondary winding coils, respectively. Similar to the case of the S/S IPT converter [24], (22) and (23) are the criteria of critical load impedance matching point for the S/SP

IPT converter to achieve maximum efficiency when operating with LIV output and ZPA input.

B. Achieving Optimum Equivalent Load Resistance

From (16) and (18), there may exist a local maximum of $R_{L,\mathrm{eq}}$, which can be calculated by solving $\frac{\mathrm{d}R_{L,\mathrm{eq}}}{\mathrm{d}R_L}=0$ and given by

$$R_{L,\mathrm{eq,max}}=\frac{1}{2\omega_H C_{S,P}},\ \text{at} \tag{24}$$

$$R_L=\frac{1}{\omega_H C_{S,P}}. \tag{25}$$

Obviously, optimum equivalent load resistance $R_{L,\mathrm{eq,opt}}$ in (22) is achievable only if

$$R_{L,\mathrm{eq,max}}>R_{L,\mathrm{eq,opt}}. \tag{26}$$

Therefore, with (22), (24), and (26), the design of μ should, therefore, satisfy

$$\mu>\mu_{\mathrm{eff}}=\sqrt{\frac{1-k^2}{1-2\,k}} \tag{27}$$

for efficiency optimization, where μ_{eff} is defined as the minimum value of μ for efficiency optimization.

Fig. 5(a) shows the equivalent load resistance $R_{L,\mathrm{eq}}$ versus the load resistance R_L under different designs of μ. μ_{eff} can be calculated as 1.36. It can be observed that when μ is less than μ_{eff}, $R_{L,\mathrm{eq}}$ cannot reach $R_{L,\mathrm{eq,opt}}$ for efficiency optimization.

C. Minimizing Equivalent Load Reactance

Supposing the optimum equivalent resistance $R_{L,\mathrm{eq,opt}}$ in (22) is achievable with proper design of μ satisfying (27), a large Q should be further achieved to minimize $\frac{\Delta X_{L,\mathrm{eq}}^2}{R_{L,\mathrm{eq}}}$ as (23). With (16), (18), and (23), the quality factor Q can be derived as

$$Q=\frac{\mu^2-1+k^2}{2k\mu^2}+\sqrt{\left(\frac{\mu^2-1+k^2}{2k\mu^2}\right)^2-1} \tag{28}$$

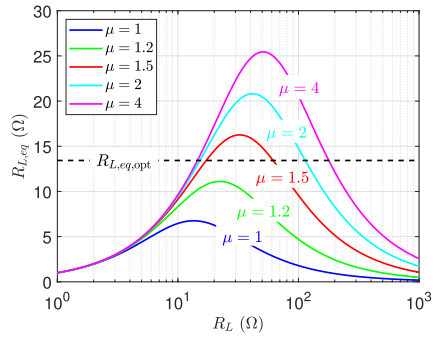
and plotted in Fig. 5(b). It can be observed that Q becomes larger with the increase of μ, which means the reactance component $\frac{\Delta X_{L,\mathrm{eq}}^2}{R_{L,\mathrm{eq}}}$ in (23) can be further minimized for higher efficiency by designing a larger value of μ.

It can be concluded that the S/SP IPT converter can achieve higher power efficiency by designing a larger value of μ. As an illustration, the operating frequency ω_H is fixed to an identical value for fair comparison, and the curves of power efficiency η versus load resistance R_L are plotted in Fig. 5(c). Compared with conventional design of unity μ, the peak efficiency is progressively improved with the increase of μ.

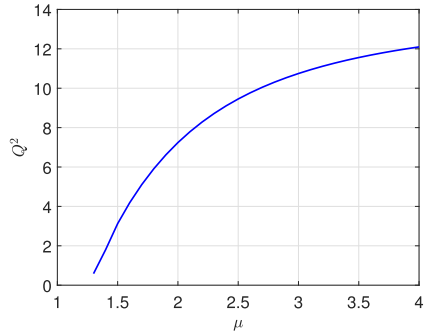
IV. Design Considerations

A. Current Stresses on the Windings

To achieve optimum efficiency, design of μ should allow equivalent load resistance $R_{L,\mathrm{eq}}$ to satisfy (22) and minimize $\Delta X_{L,\mathrm{eq}}$ toward zero as (23). $\Delta X_{L,\mathrm{eq}}$ can be ignored due to high



(a)



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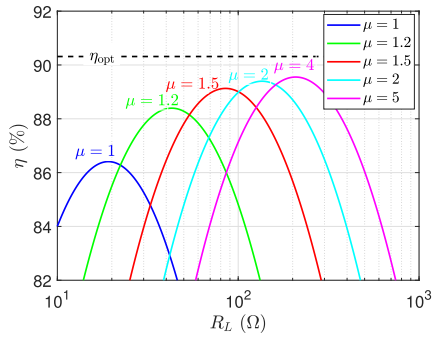

(c)

Fig. 5. Calculated results in coupling condition of $k=0.25$: (a) equivalent resistance $R_{L,eq}$ versus load resistance R_L under different designs of μ, (b) quality factor Q versus μ, and (c) power efficiency η versus load resistance R_L under different designs of μ.

quality factor Q of the resonant circuit. Therefore, for different designs satisfying (27), i.e., $\mu>\mu_{\mathrm{eff}}$, the equivalent circuit models at maximum efficiency points are nearly identical, with optimum equivalent load resistance $R_{L,eq,\mathrm{opt}}$ and negligible equivalent load reactance $\Delta X_{S,P}$ as shown in Fig. 4(b). It can be estimated that design of μ for efficiency optimization will not affect the current stresses on the primary and secondary windings too much. Such that, LIV transfer functions can be customized by designing the compensation parameters without a necessity to redesign the loosely coupled transformer. Moreover, the output power levels are almost identical under different designs of μ.

B. Compensation Capacitance Cost

It is well known that the cost of an IPT converter can be reduced by minimizing its VA rating and improving its power

efficiency [15], [16]. The S/SP IPT converter can realize ZPA input and achieve efficiency optimization by designing the compensation parameters indicated by the single factor μ discussed above. However, different designs of μ may lead to variations of overall compensation capacitance cost, which is, thus, of interest to be optimized. In general, the cost of compensation capacitor is affected by the specifications, including capacitance and voltage tolerance, but also affected by the manufacturing factors (e.g., volume) and commercial factors (e.g., order quantity, custom, or unique specifications) [25]–[27], making it infeasible to choose unique specifications for each capacitor in practice. Given identical capability of energy storage, metalized polypropylene thin film capacitors with high nominal voltage and small capacitance have better cost performance compared with those with low nominal voltage and large capacitance [25]–[27]. In addition, commercially available capacitors for high-frequency resonant converters (including IPT converters) usually have sufficiently high voltage tolerance for the compensation capacitors of the IPT converter in this work [28]. Such that, the cost of the compensation capacitance can be approximately reflected by the overall compensation capacitance.

Similar to the comparison of power efficiency, the operating frequency ω_H is fixed to an identical value under different designs of μ by choosing the compensation capacitors C_P, C_S, and $C_{S,P}$. With (1), (2), (3), (8), and (11), the compensation parameters are approximated as

$$C_P \approx \frac{1}{1-k^2}\frac{1}{\omega_H^2 L_P} \tag{29}$$

$$C_S \approx \frac{\mu^2}{1-k^2}\frac{1}{\omega_H^2 L_S}, \text{ and} \tag{30}$$

$$C_{S,P} \approx \frac{\mu^2}{\mu^2+k^2-1}\frac{1}{\omega_H^2 L_S} \tag{31}$$

with the assumption $(\mu^2-1)^2 \gg 4\,k^2\mu^2$. Overall compensation capacitance can be calculated by

$$C_{\text{total}} = C_P + C_S + C_{S,P}. \tag{32}$$

Substituting (29) to (31) into (32) and solving $\frac{\mathrm{d}C_{\text{total}}}{\mathrm{d}\mu} = 0$, design of μ for minimum capacitance is given by

$$\mu_{\text{cost}} = \sqrt{2(1-k^2)}. \tag{33}$$

As an illustration, Fig. 6 shows the compensation capacitance calculated with parameters given in Table I versus μ. A design for minimum C_{total} exists at μ_{cost}.

C. Cost-Effective Compensation Design

It has been studied in Section II that a wide range of customizable LIV outputs with ZPA input can be achieved by simply altering the compensation design indicator μ of the S/SP IPT converter. It is also revealed in Section III that the maximum efficiency $\eta_{\max}$ can be progressively enhanced with the increase of μ, and specifically $\mu > \mu_{\text{eff}}$ is required for a high efficiency. Moreover, a minimum value of overall compensation capacitance C_{total} exists at μ_{cost}, and C_{total} will increase as μ becomes larger when $\mu > \mu_{\text{cost}}$ as discussed in Section IV-C.

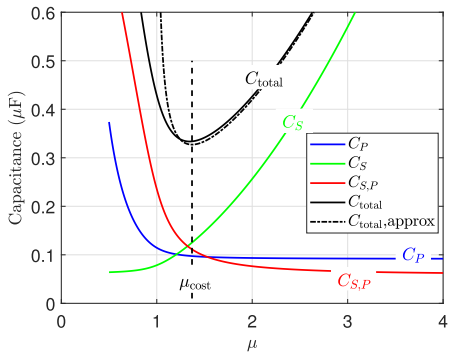

Fig. 6. Capacitance versus μ.

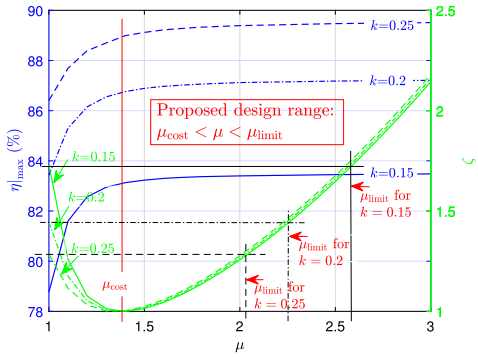

Fig. 7. Maximum efficiency $\eta_{\max}$ and normalized overall compensation capacitance ζ versus compensation design indicator μ.

Therefore, the tradeoff between improving power efficiency and minimizing overall compensation capacitance cost imposes constraints to the design range of μ for customizable LIV outputs.

The overall compensation capacitance C_{total} can be normalized as

$$\zeta = \frac{C_{\text{total}}}{C_{\text{total}}|_{\mu_{\text{cost}}}} \tag{34}$$

with the minimum value $C_{\text{total}}|_{\mu_{\text{cost}}}$ being the per-unit value. Simulation curves in Fig. 7 show how maximum efficiency $\eta_{\max}$ and normalized overall compensation capacitance ζ vary with μ. $\eta_{\max}$ increases with μ at a reducing rate (saturates as μ becomes large), and ζ increases with μ at an increasing rate when $\mu > \mu_{\text{cost}}$. Hence, increasing μ will offer diminishing return of $\eta_{\max}$ and lead to sharp increase of ζ. To achieve customizable LIV output with efficiency optimization, we may restrict ζ to be no greater than that of conventional design, i.e., $\zeta <= \zeta|_{\mu=1}$ as a cost-effective design. A limiting value of μ for ζ-restriction can be given by

$$\mu_{\text{limit}} = \sqrt{\lambda + \sqrt{\lambda^2 + k^2 + 1}} \tag{35}$$

where $\lambda = \frac{1}{2}(\frac{1}{k} + 1 + k\frac{L_S}{L_P})$. With (27) and (33), for typical conditions of coupling coefficient of wireless IPT applications, i.e., $k < 0.25$, μ_{cost} is guaranteed to be larger than μ_{eff}. Therefore, a design range of μ is proposed, given by

$$\mu_{\text{cost}} < \mu < \mu_{\text{limit}} \tag{36}$$

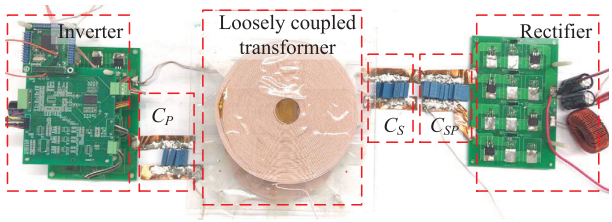

Fig. 8. Experiment setup.

TABLE II
CONVERTER PARAMETERS

Parameters	Symbols	Values
Input voltage	V_I	35 V
Filter	L_f, C_f	1.5 mH, 0.47 mF
MOSFETs	Q_1-Q_4	IPP60R165
Diodes	D_1-D_4	MBR20200
Self inductance	L_P, L_S	117.47 μH, 172.79 μH
Coil resistance	R_P, R_S	0.454 Ω, 0.626 Ω
Coupling coefficient	$k_{\min}$	0.17
	$k_{\max}$	0.254
Operating frequency	$\frac{\omega_H}{2\pi}$	50 kHz

			C_P	C_S	$C_{S,P}$
Compensation capacitance	$k_{\min}$	$\mu = 1$	104.2 nF	70.58 nF	343 nF
		$\mu = 1.35$	92.4 nF	113 nF	121 nF
		$\mu = 2$	89.54 nF	244 nF	77.8 nF
		$\mu = 2.5$	89 nF	379 nF	69.2 nF
	$k_{\max}$	$\mu = 1$	115.38 nF	78.36 nF	230.8 nF
		$\mu = 1.35$	99 nF	122 nF	113 nF
		$\mu = 2$	94 nF	255 nF	77 nF
		$\mu = 2.5$	92.4 nF	395.2 nF	68.2 nF

to achieve cost-effective compensation design of the S/SP IPT converter for customizable LIV outputs with ZPA input and optimized efficiency, as shown in Fig. 7. The range of LIV output and the percentage efficiency improvement obtained with the design of μ given in (36) should be verified as being satisfactory. Otherwise, a choice of larger μ for wider range of LIV output and better efficiency performance is required, with higher overall compensation cost ζ as compromise.

V. EXPERIMENTAL VERIFICATION

To verify the proposed cost-effective compensation design of the S/SP IPT converter, prototypes are built as shown in Fig. 8, with detailed parameters given in Table II. The S/SP converters share an identical loosely coupled transformer, where conditions of week coupling coefficient $k_{\min}$ and relatively strong coupling coefficient $k_{\max}$ will be considered to evaluate the proposed design. Various sets of C_P, C_S, and $C_{S,P}$ are used for compensation, under different compensation design indicators, i.e., $\mu = 1$, $\mu = 1.35$, $\mu = 2$, and $\mu = 2.5$. They can be calculated with (1)–(3), (8), and (11), while the practical parameters are given in Table II.

A. Measured Waveforms and LIV Outputs

Figs. 9 and 10 show the measured waveforms of the S/SP IPT converters with different compensation designs (indicated by different values of μ), at $k_{\min} = 0.17$ and $k_{\max} = 0.254$, respectively. The waveforms include the input voltage v_i, input current (primary winding current) i_P, secondary winding current i_S, and dc output voltage V_O. v_i and i_P are kept in phase, thus ZPA input can be achieved with different compensation designs of μ to minimize VA rating for the inverter. Both i_P and i_S are kept nearly identical for $\mu = 1.35$, $\mu = 2$, and $\mu = 2.5$, which coincides with the analysis in Section IV-A that current stresses on the primary winding and the secondary winding are not affected by the design of μ. It also verifies that although the output voltage and the optimum load resistance vary a lot under different designs of μ, the output power levels at maximum efficiency points are nearly identical. Thus, it is fair to compare the maximum efficiency points in Section V-B. The output voltage V_O is customizable with direct readout of the magnitude shown in Figs. 9 and 10, and the measured dc LIV transfer function

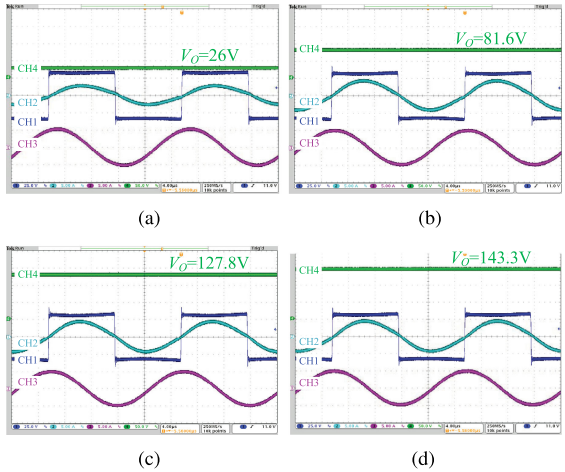

Fig. 9. Steady-state waveforms of the S/SP IPT converters at $k_{\min} = 0.17$, with different compensation deigns. CH1: v_i, 25 V/div, CH2: i_P, 5 A/div, CH3: i_S, 5 A/div, and CH4: V_O, 50 V/div. V_O can be customized from 26 to 143.3 V when the design value of μ varies from 1 to 2.5. (a) $\mu = 1$. (b) $\mu = 1.35$. (c) $\mu = 2$. (d) $\mu = 2.5$.

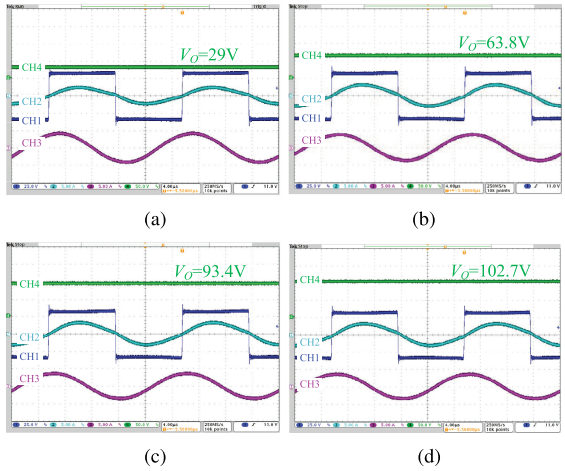

Fig. 10. Steady-state waveforms of the S/SP IPT converters at $k_{\max} = 0.254$, with different compensation deigns. CH1: v_i, 25 V/div, CH2: i_P, 5 A/div, CH3: i_S, 5 A/div, and CH4: V_O, 50 V/div. V_O can be customized from 29 to 102.7 V when the design value of μ varies from 1 to 2.5. (a) $\mu = 1$. (b) $\mu = 1.35$. (c) $\mu = 2$. (d) $\mu = 2.5$.

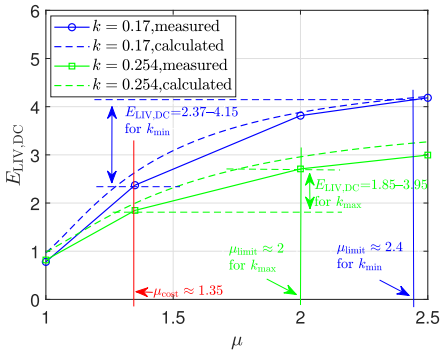

Fig. 11. Measured dc LIV transfer function $E_{\mathrm{LIV,DC}} = \frac{V_O}{V_I}$ versus compensation design indicator μ in different conditions of coupling.

$E_{\mathrm{LIV,DC}} = \frac{V_O}{V_I}$ (marked with "◯" for $k_{\min}$ and "□" for $k_{\max}$) versus μ are shown in Fig. 11. It should be noted that there exists a scale factor between the dc voltage gain and ac voltage gain, i.e., $E_{\mathrm{LIV,DC}} = \frac{8}{\pi^2} E_{\mathrm{LIV}}$. Since there exist practical converter losses, the measured dc voltage gain is slightly lower than the calculated results. However, the trend of $E_{\mathrm{LIV,DC}}$ with respect to the variation of μ coincides with the simulated results shown in Fig. 3.

B. Measured Efficiency and Overall Compensation Capacitance Cost

The input dc power and output dc power are measured by a Yokogawa PX8000 Precision Power Scope. In Fig. 12, the curves plot measured efficiency η versus load resistance R in different conditions of coupling coefficient k and with different design values of μ. The curves in dark blue indicate the efficiency performance for conventional compensation design, i.e., $\mu = 1$. Obviously, the efficiency can be enhanced with our proposed compensation design, as indicated by the direct readout of maximum efficiency points of green, red, and light blue curves, where the maximum efficiency is progressively improved with the increase of μ.

In Fig. 13, measured maximum efficiency points (marked with blue "◯" for $k_{\min}$ and blue "□" for $k_{\max}$) are plotted, which increase monotonically and saturate as μ becomes large. Although the measured maximum efficiencies are slightly lower than the simulated results shown in Fig. 7 due to the converter losses, the trend of the measured maximum efficiencies with respect to μ coincides with the simulation. The overall compensation capacitance for different designs of μ can be calculated with parameters given in Table II and the measured normalized value ζ are plotted as green curves in Fig. 13, where green "◯" and green "□" represent ζ for $k_{\min}$ and $k_{\max}$, respectively. There exist local minimums at $\mu_{\min} \approx 1.35$ for both coupling conditions, thus the overall compensation capacitance is not in a monotonic relationship with the design of μ. At $\mu_{\min} \approx 1.35$, it is great to find that there are 37% and 21.5% reduction of the over compensation capacitance as well as 5.9% and 5% improvement of the efficiency at $k_{\min}$ and $k_{\max}$, respectively, compared with

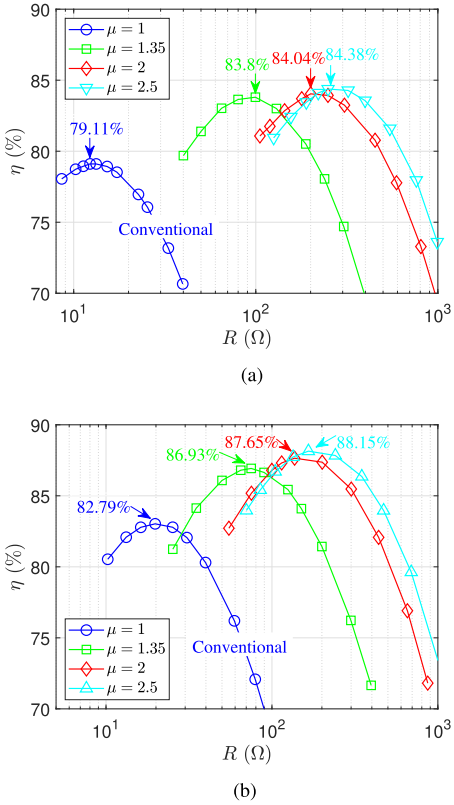

Fig. 12. Measured efficiency η versus load resistance R under different conditions of coupling coefficient. (a) $k_{\min} = 0.17$. (b) $k_{\max} = 0.254$.

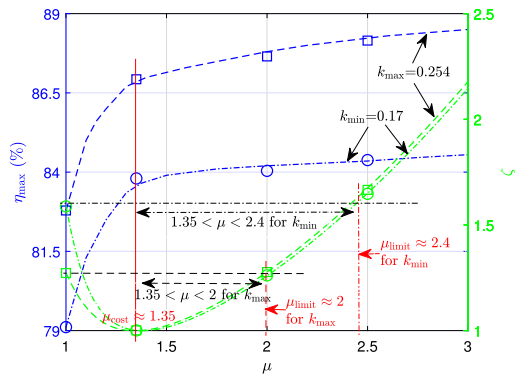

Fig. 13. Measured maximum efficiency $\eta_{\max}$ and normalized overall capacitance ζ versus compensation design indicator μ.

those with conventional design, i.e., $\mu = 1$. To achieve cost-effective compensation design for customizable LIV outputs and optimized efficiency, we restrict ζ to be no greater than $\zeta|_{\mu=1}$. Design ranges of $1.35 < \mu < 2.4$ and $1.35 < \mu < 2$ are, therefore, given for $k_{\min}$ and $k_{\max}$ as shown in Fig. 13, where $\eta_{\max}$ will be further improved and ζ will increase from its minimum but still locating in a satisfactory range. The custom ranges of LIV transfer function are shown in Fig. 11. It can also be observed in Fig. 13, beyond the proposed design ranges of μ, $\eta_{\max}$ becomes saturated while ζ increases rapidly, thus the design will not be cost-effective anymore.

TABLE III
COMPARISON OF DESIRABLE FEATURES BETWEEN OUR ARTICLE AND THE LITERATURE

Compensation Topology		No Lossy Compensation Component	Free From Transformer Parameter Constraint	LIV Output Customization	ZPA	Efficiency Enhancement
S/SP in Our paper		√	√	√	√	√
Conventional S/SP [7]–[9]		√	×	×	√	×
Basic Compensation	S/S [13]	√	×	×	×	×
	S/P [13]	√	×	×	√	×
Higher-order Compensation	LC/LC [20]	×	√	√	√	×
	LCC/LCC [21]	×	√	√	√	×
	Others [17]	×	√	√	√	×

C. Comparison With the Literature

Table III summarizes the comparison of the desirable features between our proposed design and those in the literature. All the desirable features can be achieved in our proposed design.

VI. CONCLUSION

In this article, parameters of three compensation capacitors of a S/SP IPT converter were indicated by a single factor μ, which simplifies the analysis of the relationships among compensation parameters, customizable LIV outputs with ZPA input, power efficiency, and overall compensation capacitance cost. Critical values of μ ensuring load impedance matching for optimized efficiency, achieving minimum overall compensation capacitance and limiting overall compensation capacitance for effective cost were respectively derived for guiding the design. A cost-effective compensation design achieving customizable LIV outputs with enhanced power efficiency and reduced overall compensation capacitance was elaborated. Experiment results validate the analysis and the proposed cost-effective compensation design in customizing the output and optimizing the efficiency.

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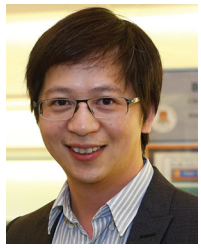

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