Non-Backflow-Power and Reduced-Switching-Loss Modulation for Bidirectional Series Resonant Converter With Wide Gain Range

Zhijian Fang, *Member, IEEE*, Haojiang Yue, Fei Xie, and Zhicong Huang, *Member, IEEE*

***Abstract*— In the achievement of high power efficiency over a wide gain range for a bidirectional series resonant converter (BSRC), conduction losses caused by backflow power and switching losses are two challenges. In this article, a novel modulation of the BSRC is proposed for a wide voltage gain range and high efficiency as well. With the proposed modulation, the BSRC can operate in both buck- and boost-like modes for a wide gain range. The resonant current is in phase with the terminal voltage on both primary and secondary sides, to eliminate the backflow power for the reduction of conduction losses. Hard turn-off problem is alleviated with a resonant current fully released before the completion of the switching cycle. Thus, the number of hard switching actions is significantly reduced compared with existing modulation schemes in the literature. A control scheme based on state-flowchart is also proposed to realize seamless transition among different working modes. To validate the proposed modulation, a 1 kVA prototype of BSRC is developed and interfaces a high-voltage bus ranging from 240 to 480 V and a low-voltage bus ranging from 24 to 56 V. Compared with conventional modulation schemes, efficiency enhancement can be observed over the whole operating range.**

***Index Terms*— Bidirectional series resonant converter (BSRC), discontinuous current mode (DCM), non-backflow-power, reduced-switching-loss, zero current switching.**

I. Introduction

BIDIRECTIONAL DC–DC converters are attracting more and more attention due to the rapid development of renewable energy sources, battery storage system, DC grids, electric vehicles (EVs), and so on. They can operate as an interface between a high-voltage bus installing energy generation devices, grid-connected converters or loads, and a low-voltage bus where energy storage devices are loaded [1]. In most of these applications, bidirectional power flow between the two buses requires high power efficiency over a wide gain range, which is still challenging the design and modulation of the DC–DC converters [2], [3], [4], [5].

Characteristics of unidirectional LLC resonant converters have been widely studied, and some studies propose bidirectional LLC resonant converters [6], [7], [8], [9]. However, in the reverse mode, the LLC resonant converter is equivalent to an LC series resonant converter, leading to a diverse gain feature compared with the forward mode. Although an auxiliary inductor can be added between the primary full-bridge circuit and the LLC resonant tank for symmetric behaviors [10], the converter suffers from the increase in power loss and component cost. Instead of using an auxiliary inductor, a resonant capacitor can be added to the secondary side of the LLC resonant tank [11], but the behaviors of the forward mode and the reverse mode are still asymmetric due to the unmatched capacitor values. Then, Jung *et al.* [12], Malan *et al.* [13], Zhang *et al.* [14], and He *et al.* [15] propose a symmetric CLLC resonant tank for the bidirectional DC–DC converter to achieve symmetric behaviors in the forward and reverse modes. The asymmetric problem can be addressed by adding proper components to the existing LLC resonant tank, but there exist obvious penalties that include the use of more components, the increase in component cost, and the decrease in power density.

With the simplest and symmetric circuit topology of the resonant tank, bidirectional series resonant converters (BSRCs) are worth investigating [16], [17], [18], [19], [20]. Compared with the CLLC resonant converter, the resonant tank of the BSRC is greatly simplified from $C_{r1}-L_{r1}-L_m-L_{r2}-C_{r2}$ to C_r-L_r, while symmetric behaviors can still be maintained by ignoring the large magnetic inductance. In general, the BSRC has four degrees of control freedom, including primary duty cycle D_p, secondary duty cycle D_s, shifting phase between the primary and the secondary φ, and switching frequency f_s. Typical modulation schemes can be configured based on these basic control variables, as highlighted in Table I for comparison.

Variable frequency modulation (VFM) changes the switching frequency f_s to regulate the output power [11], [15], [21], achieving zero voltage switching (ZVS)-ON for primary

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Zhijian Fang, Haojiang Yue, and Fei Xie are with the School of Automation, China University of Geosciences (Wuhan), Wuhan 430074, China, and also with the Hubei Key Laboratory of Advanced Control and Intelligent Automation for Complex Systems, Wuhan 430074, China (e-mail: fangjianhust@gmail.com).

Zhicong Huang is with the Shien-Ming Wu School of Intelligent Engineering, South China University of Technology, Guangzhou 510006, China (e-mail: zhiconghuang@scut.edu.cn).

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TABLE I
COMPARISON OF MODULATION SCHEMES FOR BSRC

Modulation	Control degree	Operating range	Backflow power	Soft switching	Power	Efficiency of full power output	Operating frequency
VFM [11], [15], [21]	f_s	Narrow	Medium: backflow power at input side	Good: 4 ZVS-ON and 8 ZCS-ON/OFF actions for full range	500VA	95%	73kHz-131.1kHz
PSM [13], [17], [22]	φ	Wide	Large: backflow power at both side	Medium: 8 ZVS-ON actions for high power range	200VA	95%	100kHz
PSM + PWM [23]–[31]	φ, D_p and D_s	Wide	Small: no backflow power	Poor: no more than 8 ZVS-ON actions for high power range	1000VA	95%	500kHz
VFM + PSM [18]	φ and f_s	Wide	Medium: backflow power at output side	Good: 8 ZVS-ON actions for full range	800VA	94.8%	41.3kHz
FDM [32], [33]	φ, f_s, D_p and D_s	Wide	Small: no backflow power	Medium: 8 ZVS-ON actions for high power range	1000VA	94%	100kHz
VFM + PWM (Proposed)	f_s, D_p and D_s	Wide	Small: no backflow power	Good: 14 soft-switching actions for full range	1000VA	96%	50kHz-200kHz

switches over a full operating range as shown in Fig. 1(a). However, there exists backflow power on the input side as indicated by the green area, which will increase conduction losses in the primary switches. Moreover, due to the series LC-type resonant network, the narrow operating range is another concern of VFM. To address this challenge, phase shift modulation (PSM) is proposed in some studies [13], [17], [22]. By adjusting the shifting phase φ between the primary and secondary, the output power can be regulated over a wide voltage-gain range However, two issues brought by PSM degrade the efficiency: a) soft switching cannot be maintained at light load and b) backflow power exists in both the primary and the secondary, resulting in a large circulating current.

In order to minimize the resonant current, pulsewidth modulation (PWM) of D_p and D_s is used to reduce the reactive currents, while the PSM of φ is responsible for regulating the delivered power [19], [20], [23], [24], [25]. The modulation scheme can be named as PSM + PWM. Zero voltage level can be inserted in the full-bridge circuit to block the backflow power in both the primary and the secondary to minimize the resonant current. However, the switches suffer from hard turn-on and turn-off, as shown in Fig. 1(b), resulting in significant switching losses. Some modified PWM and PSM schemes are proposed [26], [27], [28], [29], [30], [31] to reduce the switching loss, but at the cost of backflow power. Moreover, soft switching may fail in some light load conditions in these modulation schemes. Another hybrid modulation based on VFM and PSM (VFM + PSM) is proposed in [18] to achieve ZVS for the whole operating range, showing that VFM + PSM has better efficiency performance because of the reduction in the switching loss. However, the resonant current is only in phase with the terminal voltage on the primary side, which means the backflow power still exists in the secondary.

Extra control freedom can be offered by adding VFM to PSM and PWM, which can also be named as four-degrees-of-freedom modulation (FDM). Based on fundamental approximation, a complex closed-form solution of f_s, D_p, D_s, and φ can be derived for the elimination of backflow power by making the resonant current in phase with both the primary and secondary terminal voltages [32], [33]. However, a fundamental approximation cannot describe the converter features accurately when the switching frequency is away from the resonant frequency or the duty cycle is far smaller than 0.5. Therefore, in medium or light load conditions,

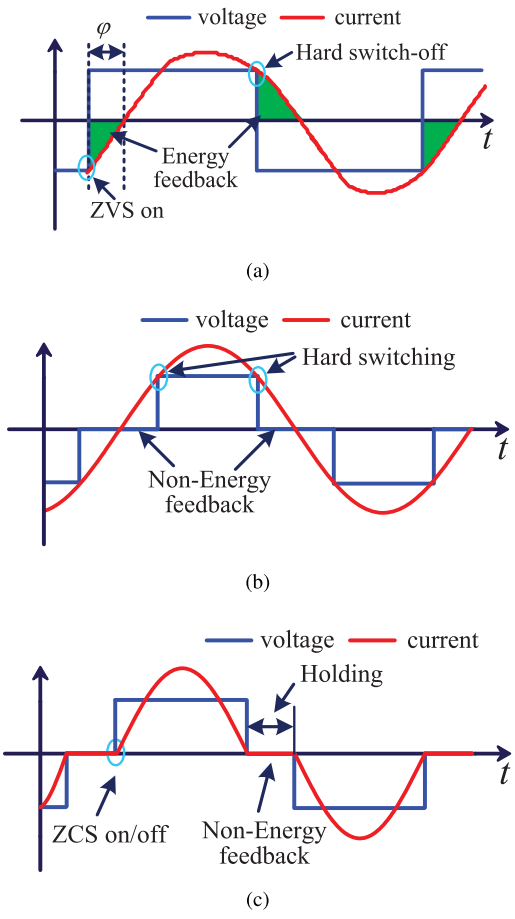


Fig. 1. Waveforms of bridge terminal voltage v_{ab} and resonant current i_r using different modulations. (a) VFM or PSM modulation. (b) PWM + PSM modulation. (c) Proposed modulation.

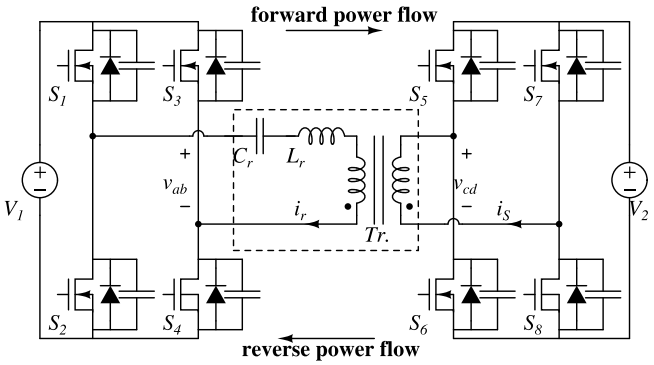


Fig. 2. Schematics of a BSRC.

backflow power cannot be eliminated. Moreover, complex calculations are used in this method to simultaneously regulate the four variables, which are difficult to be realized in practice. Therefore, the proposed method in this article only compares with the VFM + PSM method.

Although VFM + PSM can achieve ZVS turn-on, it does not take into consideration hard switching during the turn-off process, which should not be ignored especially when the turn-off current is large. Therefore, we are motivated to develop a novel modulation scheme that aims to achieve high overall efficiency with backflow power being eliminated and switching losses being optimized, as shown in Fig. 1(c).

In this article, a non-backflow-power and reduced-switching-loss modulation is proposed for the BSRC to achieve high overall efficiency within a wide gain range. The contributions of this article as follow.

1) Soft switching features are achieved not only for switch-ON but also for switch-OFF. More than 14 out of the total 16 (14/16) switching actions can realize soft switching for the full range. The number of hard switching actions is significantly reduced compared with existing modulation schemes in the literature.
2) Backflow power is both eliminated at the input and output sides.
3) Wide gain range is adjusted for the BSRC operates in buck- and boost-like modes similar to the operation of buck and boost DC–DC converters.

The rest of the article is organized as follows. Section II illustrates the proposed modulation in detail. The output characteristic and control scheme are analyzed in Section III. Section IV takes into consideration design issues on rms resonant current and soft switching. Experimental verification is given in Section V. Finally, Section VI concludes the article.

II. Proposed Modulation

As the schematic shown in Fig. 2, the BSRC consists of a primary full-bridge circuit and a secondary full-bridge circuit, interconnected with a series resonant tank ($L_r - C_r$) and a transformer. MOSFET switches $S_1 - S_4$ in the primary full-bridge circuit are modulated to generate AC voltage v_{ab} from the primary DC bus V_1. The transformer provides voltage isolation and step-down with a turn ratio of $n:1$. The secondary full-bridge circuit includes MOSFET switches $S_5 - S_8$, which are modulated to generate AC voltage v_{cd} from the secondary DC bus V_2. The magnetic inductance is large enough and the series resonant tank is considered to be insusceptible.

The proposed modulation can be divided into 8 working modes, where 4 are for the forward power flow and 4 are for the reverse power flow. The forward power flow includes Mode 1 (boost operation), Mode 2 (buck operation at high power level), Mode 3 (buck operation at medium power level), and Mode 4 (buck operation at low power level). Likewise, the reverse power flow includes Mode 5 (boost operation), Mode 6 (buck operation at high power level), Mode 7 (buck operation at medium power level), and Mode 8 (buck operation at low power level). Due to the symmetric topology of the series resonant tank, the switching patterns and waveforms are identical for the forward and reverse modes, and thus only the analysis of the forward modes, i.e., Mode 1–4, will be given in Section II. It should be noted that Modes 5–8 are dual to Mode 1–4, and thus they will not be repeated.

A. Summarized Operating States

In a half switching cycle, according to the ON/OFF states of the switches $S_1 - S_8$, six possible operating states are firstly identified and summarized in Table II. An illustration is also given as follows.

1) State A: S_1 and S_4 are ON, while D_5 and D_8 are conducting. i_r flows through the resonant tank in the forward direction. The power is fed from V_1 to V_2.

2) State B: S_2 and S_4 are ON, while D_6 and D_7 are conducting. i_r flows through the resonant tank in the reverse direction. The power is released from the resonant tank to V_2.

3) State C: S_2 and S_4 are ON, while D_5 and D_8 are conducting. i_r flows through the resonant tank in the forward direction. The power is released from the resonant tank to V_2.

4) State D: S_1, S_4, S_6, and S_8 are ON. i_r flows through the resonant tank in the forward direction. The power is released from V_1 to the resonant tank.

5) State N1 and N2: $S_5 - S_8$ are OFF. The secondary terminal of the resonant tank is open, and there is no power flow.

It can be found that the instantaneous power, flowing from the output side to the input side during the whole switching period, is nonnegative, no matter whether the state is A–D, N1 or N2. Therefore, any combination of these states can provide non-backflow-power features. In order to simplify the analysis of each working mode, all variables in the following are normalized with the base values of voltage and impedance being:

$$V_{\text{base}} = V_1 \tag{1}$$

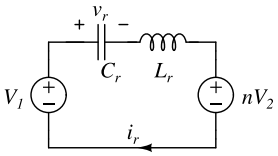
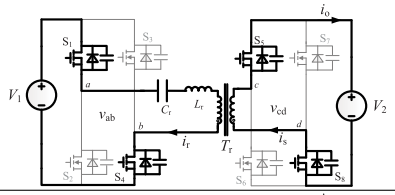
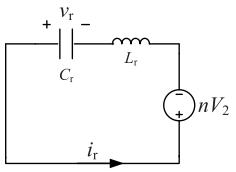
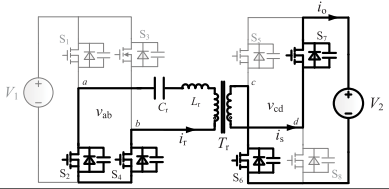
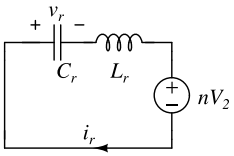
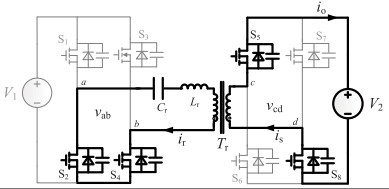
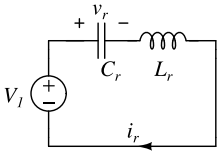
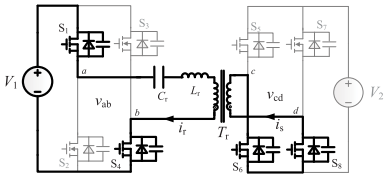
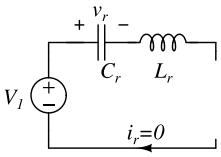
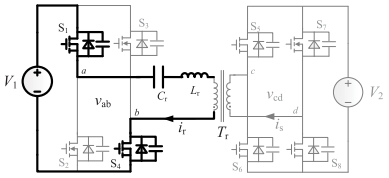
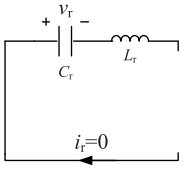
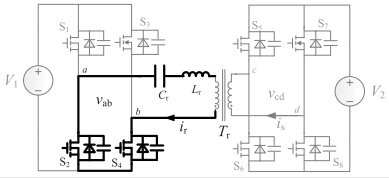
$$Z_{\text{basic}} = Z_r = \sqrt{\frac{L_r}{C_r}} \tag{2}$$

and

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{3}$$

respectively. Therefore, $M = (nV_2/V_1)$, $j_r = (i_r Z_r/V_1)$, and $m_r = (v_r/V_1)$ are defined as the normalized output voltage, resonant current and resonant voltage, respectively. $\omega_r t$ is represented by φ. And j_{ri} and m_{ri} are the instantaneous values of j_r and m_r at $\varphi_i = \omega_r t_i$.

TABLE II
SUMMARIZED OPERATING STATES OF THE BSRC

	Switches ON/OFF	Equivalent circuit	Power drawing	Function
State A	ON: S_1, S_4, D_5, D_8			Power transduction
State B	ON: S_2, S_4, D_6, D_7			Power release
State C	ON: S_2, S_4, D_5, D_8			Power release
State D	ON: S_1, S_4, S_6, S_8			Power storage
State N1	ON: S_1, S_4			Power block
State N2	ON: S_2, S_4			Power block

B. Mode 1: Boost Operation

Fig. 3 shows the switching patterns and the operating waveforms of Mode 1. There exist three stages as follows.

*1) Stage 1 ($0 \le \varphi < \varphi_1$) (**State D**):* The cycle starts with zero resonant current i_r at $\varphi = 0$, and thus S_1, S_4, S_6 and S_8 achieve ZCS-ON. v_{ab} is connected with V_1 and v_{cd} is shorted by S_6 and S_8, such that the power is stored in the resonant tank. i_r will increase sinusoidally, and the state equations are given by

$$j_r = (1 - m_{r0}) \sin \varphi \tag{4}$$

$$m_r = (-1 + m_{r0}) \cos \varphi + 1. \tag{5}$$

*2) Stage 2 ($\varphi_1 \le \varphi < \varphi_2$) (**State A**):* S_1 and S_4 are kept ON. D_5 and D_8 conduct when S_6 and S_8 are turned OFF at φ_1, which is determined by the duty cycle of secondary side D_s, donated by $\varphi_1 = 2\pi D_s$. The power is delivered from V_1 to V_2, and the state equations can be derived as follow:

$$j_r = (1 - m_{r1} - M) \sin(\varphi - \varphi_1) + j_{r1} \cos(\varphi - \varphi_1) \tag{6}$$

$$m_r = -(1 - m_{r1} - M) \cos(\varphi - \varphi_1) + j_{r1} \sin(\varphi - \varphi_1) + 1 - M. \tag{7}$$

*3) Stage 3 ($\varphi_2 \le \varphi < \pi$) (**State N1**):* j_r keeps zero and m_r maintains m_{r2} during this period since the converter is open-circuit, which could be valid only if $m_{r2} \le 1 + M$.

In Mode 1, the operation is similar to the discontinuous current mode (DCM) of a boost converter. In *Stage 1*, power is stored in the resonant tank like ON-state of the boost converter. In *Stage 2*, power is delivered from V_1 and the resonant tank to V_2 like the OFF-state of the boost converter. In *Stage 3*, power is blocked like the OFF-state of the boost converter. Similarly, D_s can be adjustable for power regulation. D_p is fixed to 0.5, and the operating frequency f_s is fixed at the resonant frequency.

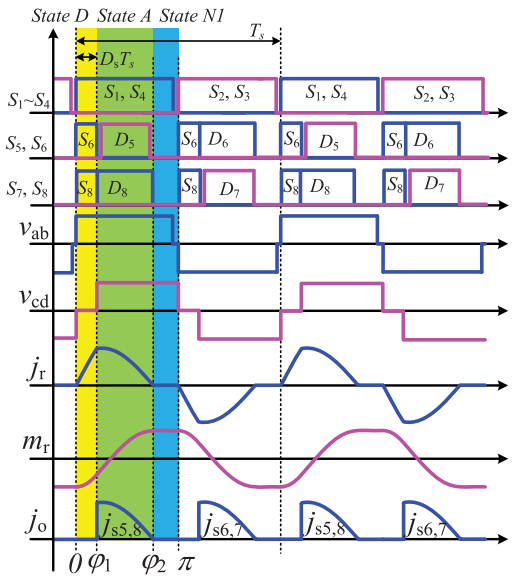


Fig. 3. Switching patterns and operating waveforms of Mode 1.

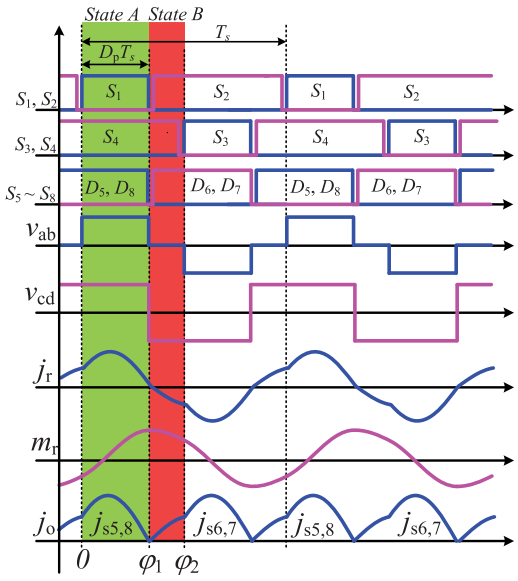


Fig. 4. Switching patterns and operating waveforms of Mode 2.

There is no backflow power between the two voltage sources in this mode. Seven of eight (7/8) switching actions are soft switching during half of the switching cycle in this mode.

C. Mode 2: Buck Operation at High Power Level

Fig. 4 shows the switching patterns and operating waveforms of the buck operation at a high power level. There exist two operating stages as follows.

*1) Stage 1 ($0 \le \varphi < \varphi_1$) (**State A**):* S_4, D_5, and D_8 are kept ON. At $\varphi = 0$, S_1 is turned ON. i_r increases sinusoidally with time to deliver power from the primary to the secondary, and it can be derived as follow:

$$j_r = (1 - m_{r0} - M)\sin\varphi + j_{r0}\cos\varphi \tag{8}$$

$$m_r = (-1 + m_{r0} + M)\cos\varphi + j_{r0}\sin\varphi + 1 - M. \tag{9}$$

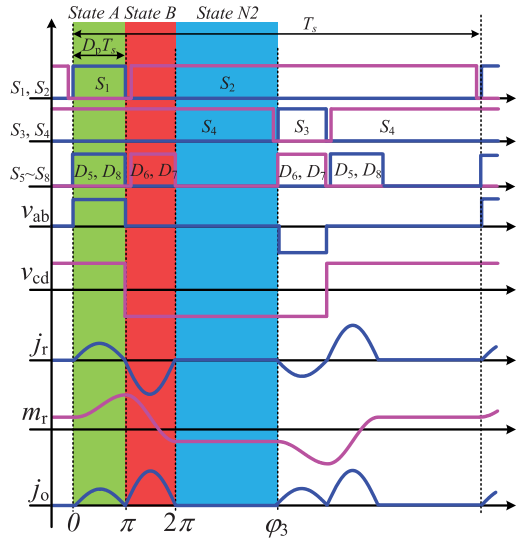


Fig. 5. Switching patterns and operating waveforms of Mode 3.

*2) Stage 2 ($\varphi_1 \le \varphi < \varphi_2$) (**State B**):* At φ_1, the resonant current i_r reaches zero, such that S_1, D_5 and D_8 are ZCS-OFF, while S_2, D_6, and D_7 are ZCS-ON. During this stage, i_r is negative and still charges V_2 to release the power stored in the resonant tank. φ_2 is $\pi f_r/f_s$, equals a half of the switching period, when S_4 turns OFF with negative current realizing ZVS-OFF. The state equations can be derived as follow:

$$j_r = (M - m_{r1})\sin(\varphi - \varphi_1) \tag{10}$$

$$m_r = (m_{r1} - M)\cos(\varphi - \varphi_1) + M. \tag{11}$$

In Mode 2, the operation is similar to a buck converter. In *Stage 1*, power is delivered from V_1 to V_2 like the ON-state of the buck converter. In *Stage 2*, the power is released from the resonant tank to V_2 like the OFF-state of the buck converter. The switching frequency f_s can be adjusted to control the amount of power delivery, like the constant-ON time control of the buck converter. The lower f_s, the smaller amount of power is delivered. f_s ranges from f_r to $(f_r/2)$, i.e., $(f_r/2) \le f_s \le f_r$ in this operation. There is no backflow power, thus decreasing the resonant current. Seven of eight (7/8) switching actions are soft switching during half of the switching cycle in this mode.

D. Mode 3: Buck Operation at Medium Power Level

The delivered power decreases with the decrease of the switching frequency. When the switching frequency is smaller than half of the resonant frequency, i.e., $f_s < (f_r/2)$, the converter operates at Mode 3. Fig. 5 shows the switching patterns and operating waveforms. There exists three operation stages as follows.

*1) Stage 1 ($0 \le \varphi < \pi$) (**State A**):* At $\varphi = 0$, i_r rises from zero, and thus S_1, D_5 and D_8 are ZCS-ON. S_4 is kept ON. This mode ends when i_r reaches zero again at $\varphi = \pi$, which is about half of the resonant period. The state equations can be derived as follow:

$$j_r = (1 - m_{r0} - M)\sin\varphi \tag{12}$$

$$m_r = (-1 + m_{r0} + M)\cos\varphi + 1 - M. \tag{13}$$

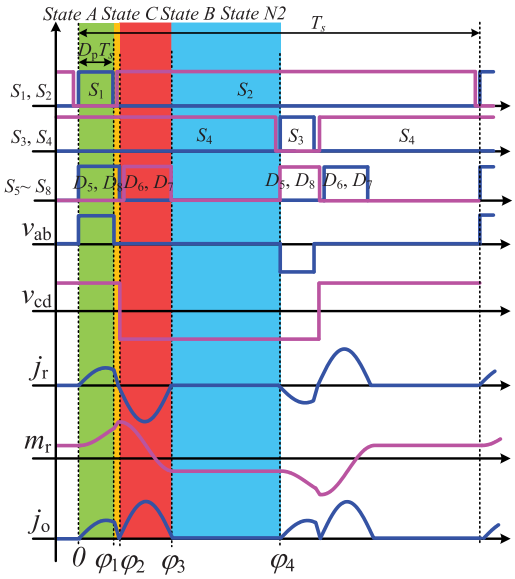


Fig. 6. Switching patterns and operating waveforms of Mode 4.

*2) Stage 2 ($\pi \le \varphi < 2\pi$) (**State B**):* i_r reaches zero again at $\varphi = \pi$. S_1, D_5, and D_8 are ZCS-OFF, while S_2, D_6, and D_7 are ZCS-ON. During this stage, since i_r is negative, it charges V_2 through S_6 and S_7 and releases the power stored in the resonant tank, given by

$$j_r = (M - m_{r1}) \sin(\varphi - \pi) \tag{14}$$

$$m_r = (m_{r1} - M) \cos(\varphi - \pi) + M. \tag{15}$$

*3) Stage 3 ($2\pi \le \varphi < \varphi_3$) (**State N2**):* At $\varphi = 2\pi$, i_r reaches zero, and thus D_6 and D_7 are ZCS-OFF. Then, the output circuit is shut OFF to block the low voltage V_2, and i_r is maintained to zero until the next half cycle, where $\varphi_3 = \pi f_r / f_s$. This stage could happen only when $m_{r2} \ge -M$.

The Mode 3 is similar to the DCM of the buck converter. In *Stage 1*, power is transferred from V_1 to V_2 like the ON-state of the buck converter. *Stage 2* is like the OFF-state with circulating current, while *Stage 3* is like the OFF-state without circulating current. *Stage 1* and *Stage 2* occupy a half resonant cycle, to realize soft switching. The delivered power can be regulated by f_s, ranging from $f_{\min}$ to $f_r/2$, where $f_{\min}$ is the minimum switching frequency of the converter. The delivered power decreases with the decrease of f_s. In this mode, there is no backflow power, and all switches achieve ZCS-ON and ZCS-OFF.

E. Mode 4: Buck Operation at Low Power Level

When the switching frequency reaches the minimum value, i.e., $f_s = f_{\min}$, the converter operates at a low power level, as shown in Fig. 6. The switching frequency is fixed to $f_{\min}$, and duty cycle D_p of upper switches S_1 and S_3 is controlled to regulate the delivered power. There exist four stages as follows.

*1) Stage 1 ($0 \le \varphi < \varphi_1$) (**State A**):* Since i_r is discontinuous at this stage, i_r starts rising from zero at $\varphi = 0$. S_1, D_5 and D_8 are ZCS-ON. This stage ends at $\varphi_1 = 2\pi f_r / f_{\min} D_p$, where D_p is adjusted for power regulation. The state equations can be derived as follow:

$$j_r = (1 - m_{r0} - M) \sin\varphi \tag{16}$$

$$m_r = (-1 + m_{r0} + M) \cos\varphi + 1 - M. \tag{17}$$

*2) Stage 2 ($\varphi_1 \le \varphi < \varphi_2$) (**State C**):* At φ_1, S_1 is turned OFF. i_r flows through D_2, making S_2 ZVS-ON. The power stored in the resonant tank is released to V_2. The state equations can be derived as follow:

$$j_r = (-M - m_{r1}) \sin(\varphi - \varphi_1) + j_{r1} \cos(\varphi - \varphi_1) \tag{18}$$

$$m_r = (m_{r1} + M) \cos(\varphi - \varphi_1) + j_{r1} \sin(\varphi - \varphi_1) - M. \tag{19}$$

*3) Stage 3 ($\varphi_2 \le \varphi < \varphi_3$) (**State B**):* At φ_2, i_r reaches zero again. Thus, D_5 and D_8 are ZCS-OFF. The state equations can be derived as follow:

$$j_r = (M - m_{r2}) \sin(\varphi - \varphi_2) \tag{20}$$

$$m_r = (m_{r2} - M) \cos(\varphi - \varphi_2) + M \tag{21}$$

i_r charges V_2 to release the power stored in the resonant tank. And this period could work for half resonant cycle.

*4) Stage 4 ($\varphi_3 \le \varphi < \varphi_4$) (**State N2**):* i_r is discontinuous from φ_3 to φ_4. D_6 and D_7 are ZCS-OFF. The output circuit stops working. i_r maintains null until the next half cycle, which could occur only if $m_{r3} \ge -M$.

The Mode 4 is also similar to the DCM of a buck converter. *Stage 1* is like the ON-state, *Stage 2* and *Stage 3* are like the OFF-state with circulating current, and *Stage 4* is like the OFF-state without circulating current. Since f_s is fixed to $f_{\min}$, D_p is regulated to control the delivered power. Smaller D_p contributes to lowering the delivered power. There is no backflow power in this mode. Seven of eight (7/8) switching actions are soft switching during half of the switching cycle.

III. Output Characteristic and Control Scheme

A. Analysis of Output Characteristic

Based on the modulation scheme proposed in Section II, the control variables for the four working modes (forward power flow as an example) are not identical. In Mode 1, D_s is controlled for output power regulation. f_s is responsible for Modes 2 and 3, while D_p takes charge of Mode 4.

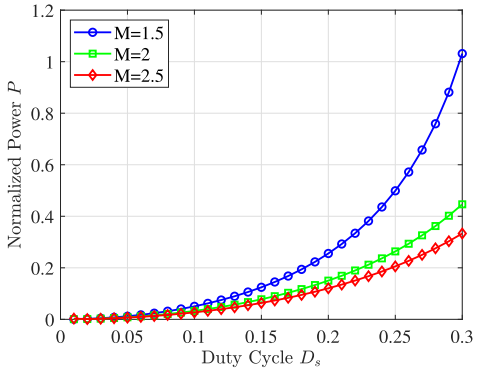
With the state equations derived in Section II, an accurate model can be built for the BSRC to analyze the output characteristic. It is noteworthy that, it is difficult to get analytical solutions to these nonlinear equations, and alternatively a numerical way with the help of MATLAB is used in this article [34]. The boundary conditions are highlighted in Appendix. Table III summarizes the corresponding control variables as well as their range for each working mode. The curves of output power versus control variables for different working modes are depicted in Fig. 7 and illustrated as follows.

1) Mode 1: The switching frequency is fixed as $f_s = f_r$, while the conducting time D_sT_s of S_6 and S_8 is controlled to regulate the output power. Curves plotted in Fig. 7(a) show the normalized delivered power versus the duty cycle D_s under different voltage gain M. As shown in Table III, D_s varies from 0 to $D_{s,\max}$ to regulate the output power ranging from 0 to $P_{\max}$, which is the maximum power calculated in

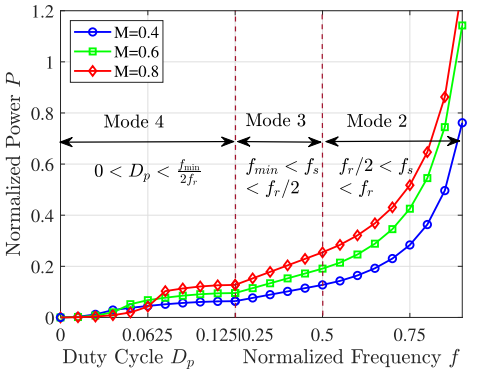
TABLE III
CONTROL VARIABLE AND ITS RANGE FOR EACH WORKING MODE

	f_s	D_p	D_s	P
Mode 1	f_r	0.5	$[0,\ D_{s,\max}]$	$[0,\ P_{\max}]$
Mode 2	$[0.5f_r,\ f_r]$	$[0.25,\ 0.5]$	0	$[P_1, +\infty)$
Mode 3	$[f_{\min},\ 0.5f_r]$	$[\frac{f_{\min}}{2f_r},\ 0.25]$	0	$[P_2,\ P_1]$
Mode 4	$f_{\min}$	$[0,\ \frac{f_{\min}}{2f_r}]$	0	$[0,\ P_2]$

[1] $P_1 = \frac{nV_1V_2}{\pi Z_r}$, $P_2 = \frac{2nV_1V_2f_{\min}}{\pi Z_r f_r}$.



(a)



(b)

Fig. 7. Normalized power against the duty cycle and switching frequency with the proposed modulation scheme. (a) Boost operation (Mode 1). (b) Buck operation (Mode 2–4).

Section IV-B. The delivered power increases with the increase of D_s.

2) Mode 2: D_s is fixed at 0, and f_s is controlled to regulate the output power. D_p is determined by f_s according to (A.15). Curves plotted in Fig. 7(b) show the normalized delivered power versus the switching frequency f_s under different voltage gain M. As shown in Table III, f_s varies from $0.5f_r$ to f_r to regulate the output power ranging from P_1 to infinity. Correspondingly, D_p varies from 0.25 to 0.5. The delivered power increases with the increase of f_s.

3) Mode 3: D_s is fixed at 0, and f_s is controlled to regulate the output power. Unlike that in Mode 2, D_p is determined by f_s according to (A.20). Curves plotted in Fig. 7(b) show the normalized delivered power versus the switching frequency f_s under different voltage gain M. As shown in Table III, f_s varies from $f_{\min}$ to $0.5f_r$ to regulate the output power ranging from P_2 to P_1. Correspondingly, D_p varies from $(f_{\min}/2f_r)$ to 0.25. The delivered power increases with the increase of f_s.

4) Mode 4: D_s and f_s are fixed at 0 and $f_{\min}$, respectively. D_p is controlled to regulate the output power. Curves plotted in Fig. 7(b) show the normalized delivered power versus the duty cycle D_p under different voltage gain M. As shown in Table III, D_p varies from 0 to $(f_{\min}/2f_r)$ to regulate the output power ranging from 0 to P_2. The delivered power increases with the increase of D_p.

It can be observed from Table III and Fig. 7 that, the control variables, D_s, D_p, and f_s, can continuously vary to regulate the delivered power among different working modes.

B. Control Scheme

Based on the analysis in Section III-A, each working mode has an identical modulation scheme and output characteristic. The controller design first begins with power regulation in each working mode, as shown in Fig. 8. In this case, V_2 is controlled to track $V_{2\text{ref}}$ for forward and reverse power flow conditions. Similarly, V_1 also can be regulated to track $V_{1\text{ref}}$.

1) In Mode 1, f_s and D_p are fixed at f_r and 0.5, respectively. D_s is controlled for power regulation.
2) In Mode 2, f_s is regulated to control the power, and D_p is correlatively determined by f_s based on (A.15). D_s keeps zero.
3) In Mode 3, f_s is kept controlled, and D_p is correlatively determined by f_s according to (A.20).
4) In Mode 4, D_p is regulated to control the power with a fixed minimum switching frequency $f_{\min}$.

Moreover, since the output power has a monotonic relationship with the corresponding control variable in all the working modes, simple PI controllers can be used.

Then, the seamless switchover between the working modes is based on a state flowchart, as shown in Fig. 9. P is defined as positive when the power is delivered from V_1 to nV_2. The initial state is determined by the output voltage V_2, the desired output voltage value $V_{2\text{ref}}$ and voltage gain $M = nV_2/V_1$. The criteria are given as follows.

1) If $M \le 1$ and $V_{2\text{ref}} \ge V_2$, converter enters into Mode 2.
2) If $M \le 1$ and $V_{2\text{ref}} < V_2$, converter enters into Mode 5.
3) If $M > 1$ and $V_{2\text{ref}} \ge V_2$, converter enters into Mode 1.
4) If $M > 1$ and $V_{2\text{ref}} < V_2$, converter enters into Mode 6.

The rest operating principle of the state flowchart can be detailed as follows.

1) In Mode 1, if $D_s \le 0$ & $V_2 > V_{2\text{ref}}$ & $P > 0$, the BSRC jumps to Mode 2 through path ①. However, if $V_2 > V_{2\text{ref}}$ & $D_s \le 0$ & $P \le 0$, the BSRC reverses the power flow direction and jumps to Mode 8 via path ⑨. Unless specified otherwise.
2) In Mode 2, when $f_s \le f_r/2$, the BSRC jumps to Mode 3 through path ②. But if $f_s \ge f_r$ & $V_2 < V_{2\text{ref}}$, the BSRC jumps back to Mode 1 through path ⑯.
3) In Mode 3, when f_s is below $f_{\min}$, the BSRC jumps to Mode 4 through path ③. But if f_s is above $f_r/2$, the BSRC jumps back to Mode 2 via path ⑮.
4) In Mode 4, when $V_2 > V_{2\text{ref}}$ & $D_p \le 0$ & $P \le 0$, the BSRC reverses the power flow direction and works at Mode 5 via path ④. But if the duty cycle D_p is

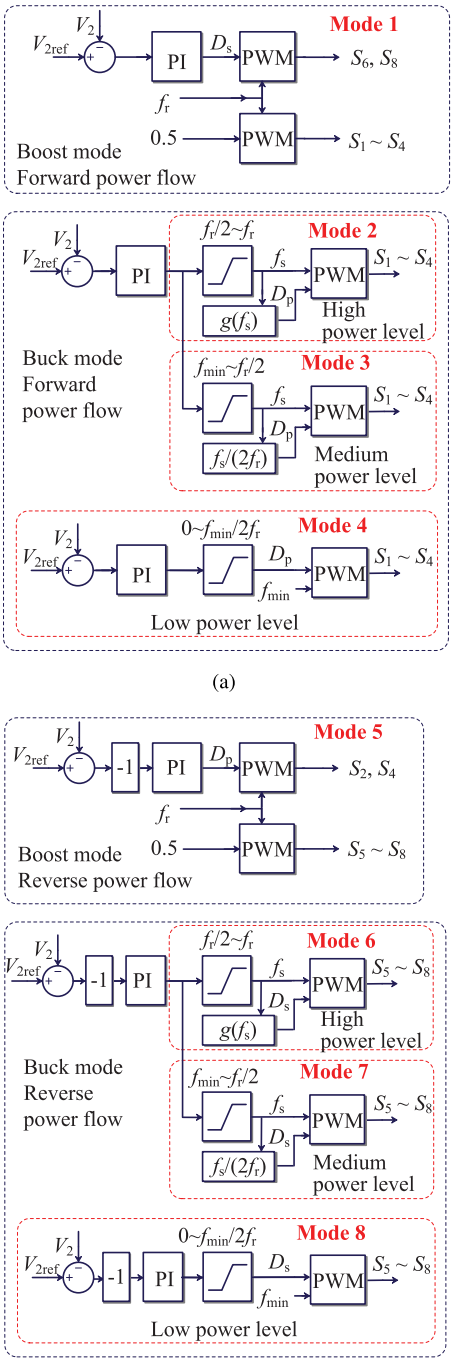


Fig. 8. Controller for power regulation in each working mode. (a) Forward and (b) reverse power flow.

increased to be above $f_{min}/2f_r$ for more output power, the BSRC jumps back to Mode 3 through path ⑭.

In order to make the control variables seamless transfer among different working modes, when the converter enters a new working mode, it is not necessary to start the controller from an initialized state. The initial values of the controllers in the "ready-to-go" working modes will also be updated with the controller in the currently "in-use" working mode. Thus the output power, switching frequency, and duty cycle are continuously regulated.

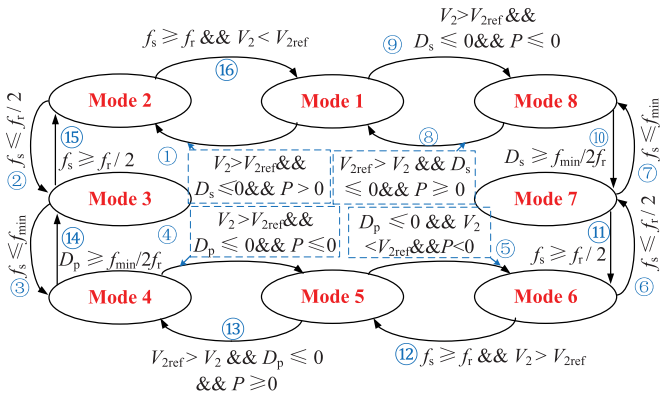


Fig. 9. State flowchart for working mode switchover.

IV. RMS Resonant Current and Soft Switching

A. rms Resonant Current

In order to evaluate the rms resonant current of the proposed modulation method, the rms value of i_r in the article is compared between different modulations since the conduction loss is only associated with the rms current in the switches and the transformer. Then the normalized rms value of i_r is represented as follows:

$$j_{r,\mathrm{rms}} = \frac{i_{r,\mathrm{rms}}}{I_1} \tag{22}$$

where I_1 is the input current that can be calculated by

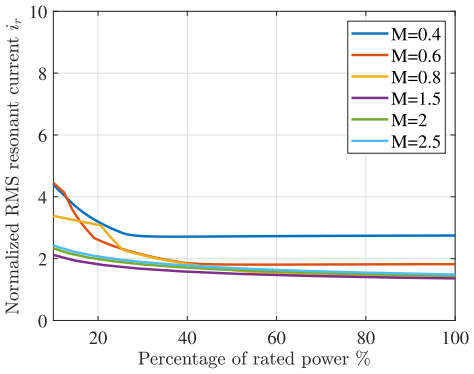
$$I_1 = \begin{cases} \dfrac{2}{T_s}\displaystyle\int_{t_0}^{t_2} i_r \mathrm{d}t, & \text{for Mode 1} \quad (23a) \\ \dfrac{2}{T_s}\displaystyle\int_{t_0}^{t_1} i_r \mathrm{d}t, & \text{for Mode 2}\sim 4 \quad (23b) \end{cases}$$

$i_{r,\mathrm{rms}}$ is the rms value of resonant current. $j_{r,\mathrm{rms}}$ can represent the conduction loss of the converter for delivering the same power. Larger $j_{r,\mathrm{rms}}$ means larger conduction losses.

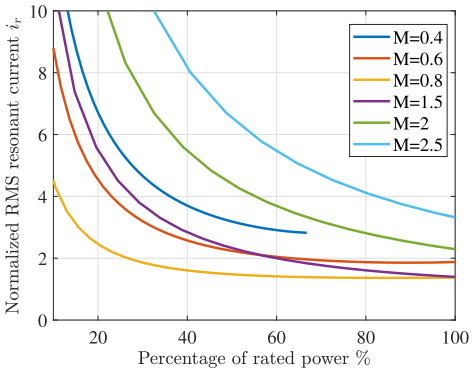
In order to verify the proposed method, the analytical and simulated rms resonant current curves with respect to the delivered power for different voltage gain are plotted in Fig. 10. As the figure shows, the normalized rms values could decrease with respect to the increase of the delivered power. And when the voltage gain is close to 1, the normalized rms value could fall. The normalized rms value of the proposed modulation is observably lower than the other two modulations, PSM and VFM + PSM. This means the conduction losses of the proposed modulation can be reduced due to non-backflow-power. The same conclusion is also given in [30] and [31]. In particular, D_5–D_8 are uncontrolled rectification in the proposed modulation. However, S_5–S_8 for VFM + PSM method realize synchronous rectification (SR) resulting in small conduction loss. When SR is implemented in the proposed modulation, the conduction loss can be further reduced as well.

B. Critical Conditions for Soft Switching

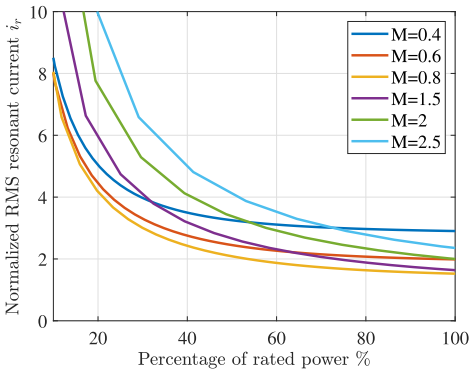
Critical conditions for soft switching under all the working modes (forward power flow as an example) are analyzed as follows.



(a)



(b)



(c)

Fig. 10. Curves of normalized rms resonant current versus delivered power with different modulations. (a) Proposed, (b) PSM, and (c) VFM + PSM modulation.

1) Mode 1: Based on the operating principle of Mode 1 illustrated in Section II-B, i_r should be positive at φ_1, while it should keep zero during $\varphi_2 \sim \pi$. Thus, the critical condition of soft switching in Mode 1 can be derived as follow:

$$m_{r2} < 1 + M \tag{24}$$

and

$$j_{r1} \geq 0. \tag{25}$$

With the mode solver demonstrated in Appendix, Fig. 11 plots the normalized output current J_o versus the normalized output voltage M when $m_{r2} = 1 + M$. To satisfy (24), the BSRC should operate in the area below the curve. The maximum normalized output current can be readily achieved

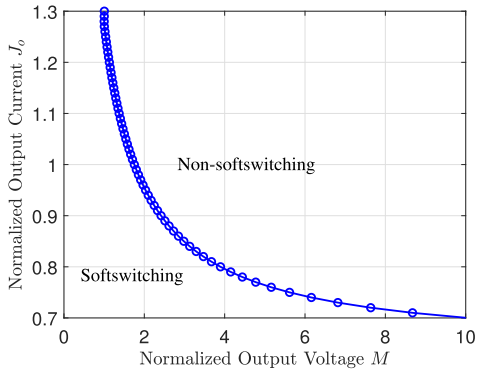


Fig. 11. Boundary of soft switching in Mode 1.

from the curve, donated by $J_{o,\max}$. Within the operating region, the delivered power should not be over $P_{\max} = J_{o,\max} M V_1^2 / Z_r$.

With (A.1), j_{r1} can be rewritten as follow:

$$j_{r1} = (1 - m_{r0}) \sin \varphi_1 \tag{26}$$

where $0 \leq \varphi_1 < \pi$. Thus $\sin \varphi_1 \geq 0$. Since the peak value of resonant voltage $|m_{r0}|$ increase with power, $m_{r0} = 0$ is the maximum value at $D_s = 0$, when $|m_{r0}|$ reaches the minimum value. Such that, $1 - m_{r0} \geq 1$, and (25) can be always satisfied in Mode 1.

In brief, when $P \leq P_{\max}$, the BSRC can realize soft switching in Mode 1.

2) Mode 2: Based on the operating principle of Mode 2 illustrated in Section II-C, i_r should keep zero at φ_1, while it should be positive at 0. Thus, the critical condition of soft switching at Mode 2 can be derived as follow:

$$j_{r1} = 0 \tag{27}$$

and

$$j_{r0} > 0. \tag{28}$$

Equation (27) is the constrain condition for Mode 2, as given in (A.6). The duty cycle D_p complies with (A.15) to satisfy (27). With (A.12), j_{r0} can be rewritten as follow:

$$j_{r0} = -\frac{\sin \varphi_1 \sin (\varphi_2 - \varphi_1)}{\sin \varphi_2}. \tag{29}$$

Since $j_{r2} = -j_{r0}$ and $\pi \leq \varphi_2 \leq 2\pi$ for $f_r \geq f_s \geq 0.5 f_r$, there only exists a zero-cross point φ_1 during 0 to φ_2. Then $0 < \varphi_1 < \pi$, and $0 < (\varphi_2 - \varphi_1) < \pi$. Such that, (28) can always be satisfied in Mode 2.

In brief, if D_p complies with (A.15), the BSRC can achieve soft switching in Mode 2 without sensing i_r.

3) Mode 3: Based on the operating principle of Mode 3 illustrated in Section II-D, i_r should be zero at 0, φ_1 and φ_2. Since φ_1 and φ_2 are the half and one resonant cycle, respectively, only if i_r is zero at 0, the BSRC can realize soft switching. Thus i_r should be discontinuous, and the critical condition of soft switching in Mode 3 can be derived as follow:

$$m_{r2} \geq -M. \tag{30}$$

Based on (A.19), m_{r2} can be rewritten as follow:

$$m_{r2} = 2M - 1. \tag{31}$$

Thus, when the following inequality is satisfied, the BSRC can achieve soft switching in Mode 3

$$\frac{1}{3} \le M \le 1. \tag{32}$$

4) Mode 4: Based on the operating principle of Mode 4 illustrated in Section II-E, i_r is zero at 0, φ_2 and φ_3. Due to the natural commutation, $i_{r2} = 0$ and $i_{r3} = 0$ can be obtained. To satisfy $i_{r0} = 0$, i_r should be discontinuous. Meanwhile, ZVS-ON of S_2, S_4 can be achieved only when $i_r > 0$ at φ_1. Thus, the critical condition of soft switching in Mode 4 can be derived as follow:

$$m_{r3} \ge -M \tag{33}$$

and

$$j_{r1} > 0. \tag{34}$$

Since m_{r3} decreases with the increase of delivered power, the minimum value of m_{r3} in Mode 4 is $2M - 1$, when $D_p = (f_{\min}/2f_r)$. To satisfy (33), $M > (1/3)$ should be satisfied. With (A.21), the minimum value of j_{r1} can be written as follow:

$$j_{r1,\min} = (1 + m_{r3,\min} - M)\sin\varphi_1 = M\sin\varphi_1. \tag{35}$$

Thus, (34) can always be satisfied.

In brief, if $(1/3) \le M \le 1$, the BSRC can achieve soft switching in Mode 4.

In conclusion, based on the analysis of critical conditions for soft switching in the four working modes, the intersected critical conditions for soft switching can be highlighted as follow:

$$P \le P_{\max}, \quad \text{for Mode 1} \tag{36}$$

$$M \ge \frac{1}{3}, \quad \text{for Mode 2, 3, and 4.} \tag{37}$$

Once (36) and (37) are both satisfied via the design of resonant tank Z_r and transformer n, soft switching can be achieved for the wide operating range.

C. Summary of Switching Loss

The switching features for the proposed modulation are summarized in Table IV. In general, there are 8 switches in the BSRC, and thus each switching cycle includes 16 switching actions. For the conventional VFM + PSM [18], although 8 turn-on actions realize soft switching, the other 8 turn-off actions suffer from hard switching that cannot be ignored especially when there exists large turn-off current. It can be observed that 14 of the total 16 switching actions are soft-switching in Mode 1, Mode 2, and Mode 4. Moreover, all switching actions are soft switching in Mode 3. Due to the switch capacitance, there is still ZCS-OFF loss, which is given as follows:

$$P_{\mathrm{ZCS_{on}}} = \frac{1}{2}C_{\mathrm{ds}}V_{\mathrm{dc}}^2. \tag{38}$$

V_{dc} is the DC voltage and C_{ds} is the drain–source capacitance of the switches.

TABLE IV
SOFT SWITCHING FEATURES OF THE PROPOSED MODULATION SCHEME

		Boost mode	Buck mode		
		Mode 1	Mode 2	Mode 3	Mode 4
S_1	Turn on	ZCS	non-ZCS	ZCS	ZCS
	Turn off	ZCS	ZCS	ZCS	non-ZCS
S_2	Turn on	ZCS	ZCS	ZCS	ZVS
	Turn off	ZCS	ZVS	ZCS	ZCS
S_3	Turn on	ZCS	non-ZCS	ZCS	ZCS
	Turn off	ZCS	ZCS	ZCS	non-ZCS
S_4	Turn on	ZCS	ZCS	ZCS	ZVS
	Turn off	ZCS	ZVS	ZCS	ZCS
S_5	Turn on	ZVS	ZCS	ZCS	ZCS
	Turn off	ZCS	ZCS	ZCS	ZCS
S_6	Turn on	ZCS	ZCS	ZCS	ZCS
	Turn off	non-ZCS	ZCS	ZCS	ZCS
S_7	Turn on	ZVS	ZCS	ZCS	ZCS
	Turn off	ZCS	ZCS	ZCS	ZCS
S_8	Turn on	ZCS	ZCS	ZCS	ZCS
	Turn off	non-ZCS	ZCS	ZCS	ZCS
Soft switching		14/16	14/16	16/16	14/16

For the conventional methods with single ZVS-ON and hard-OFF, the ZVS-ON loss is eliminated but large hard-OFF loss appears, which is

$$P_{\text{hard OFF}} = \frac{1}{2}V_{\mathrm{dc}}i_{\mathrm{OFF}}t_{\mathrm{OFF}}f_s \tag{39}$$

where i_{OFF} is the turning OFF current and t_{OFF} is the switching falling time. As the analysis in Section I, i_{OFF} could be very large, especially in light load conditions. Thus the total switching loss could be very large in the modulations with single ZVS-ON and hard-OFF. The comparison between the conventional methods with single ZVS-ON and hard-OFF and ZCS-ON/OFF method has also given in [38], which verifies that the ZCS-ON/OFF has efficiency advantages over conventional sole ZVS-ON and hard-OFF.

Therefore, in the first place, the proposed modulation cures the problem of hard turn-off loss by reducing the number of hard switching actions. In the second place, with the proposed modulation, the magnitude of the turn-off current is significantly reduced compared with the conventional VFM + PSM, as shown in Fig. 12. Such that, the problem of the turn-off loss can be further alleviated.

V. EXPERIMENTAL VERIFICATION

As shown in Fig. 13, a 1 kVA experimental prototype of the BSRC is built with specifications and parameters given in Table V. The magnetic devices are designed according to $0.5f_r = 100$ kHz. Because when magnetic current i_m is zero, the magnetic flux density B could be fixed, and no magnetic loss could appear. In the proposed modulation, the longest conduction time of resonant current i_r is $2T_r$ for all the operation modes as shown in Figs. 3–6, i_r is zero during other times, as well as magnetic current. The minimum varying frequency of i_m is $0.5f_r$.

A. Measured Operating Waveforms

Typical operating waveforms of the BSRC in the forward mode and the reverse mode are shown in Figs. 14 and 15,

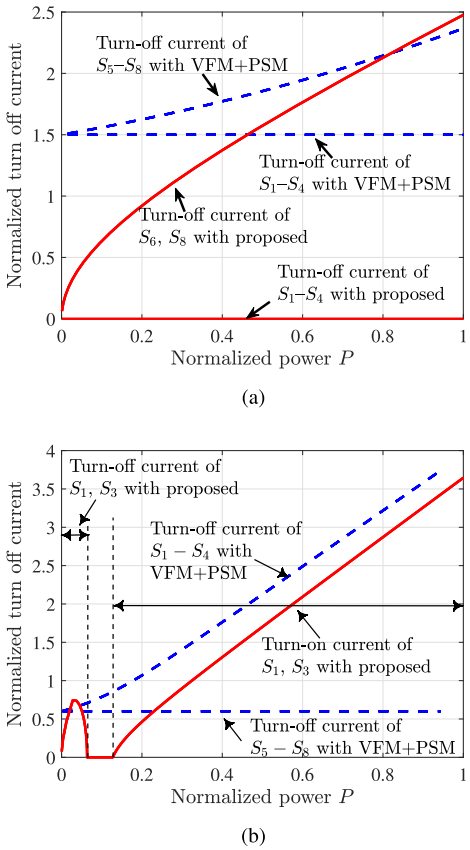


Fig. 12. Turning current of proposed modulation versus VFM + PSM modulation. (a) $M = 2.5$ in the boost operation (Mode 1). (b) $M = 0.4$ in the Buck operation (Mode 2–4).

TABLE V
SPECIFICATIONS AND PARAMETERS OF THE BSRC

Specifications		Symbols	Values
Primary side	Voltage range	V_1	240 – 480 V
	Nominal voltage	$V_{1,\text{nom}}$	400 V
	Current range	I_1	0 – 2.5 A
Secondary side	Voltage range	V_2	24 – 56 V
	Nominal voltage	$V_{2,\text{nom}}$	48 V
	Current range	I_2	0 – 20 A

Parameters	Symbols	Values
Primary-side switches	$S_1 - S_4$	E3M0065090D
Secondary-side switches	$S_5 - S_8$	E3MIPP030N10N5D
Resonant inductor	L_r	50 μH
Resonant capacitor	C_r	12 nF
Resonant frequency	f_r	200 kHz
Turn ratio	n	16:2
Switching frequency	f_s	50 – 200 kHz

respectively. Since the forward mode and the reverse mode are symmetric, only an illustration of the operating waveforms in the forward mode is performed as follows.

For Modes 2–4, the normalized gain M is 0.4 with the input voltage being 480 V and the output voltage being 24 V. In Mode 2, the switching frequency is about 110 kHz which is between the resonant frequency 200 kHz and half of the resonant frequency 100 kHz. As shown in Fig. 14(a), S_2 and S_4 are turned OFF when i_r flows through the anti-parallel diodes, and turned ON when $i_r = 0$, thus realizing zero loss switching. As the complements of S_2 and S_4, S_1 and S_3 realize ZCS-OFF but suffer from hard turn-on. S_5–S_8 operate

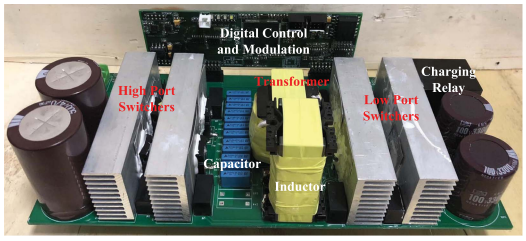


Fig. 13. Experimental prototype.

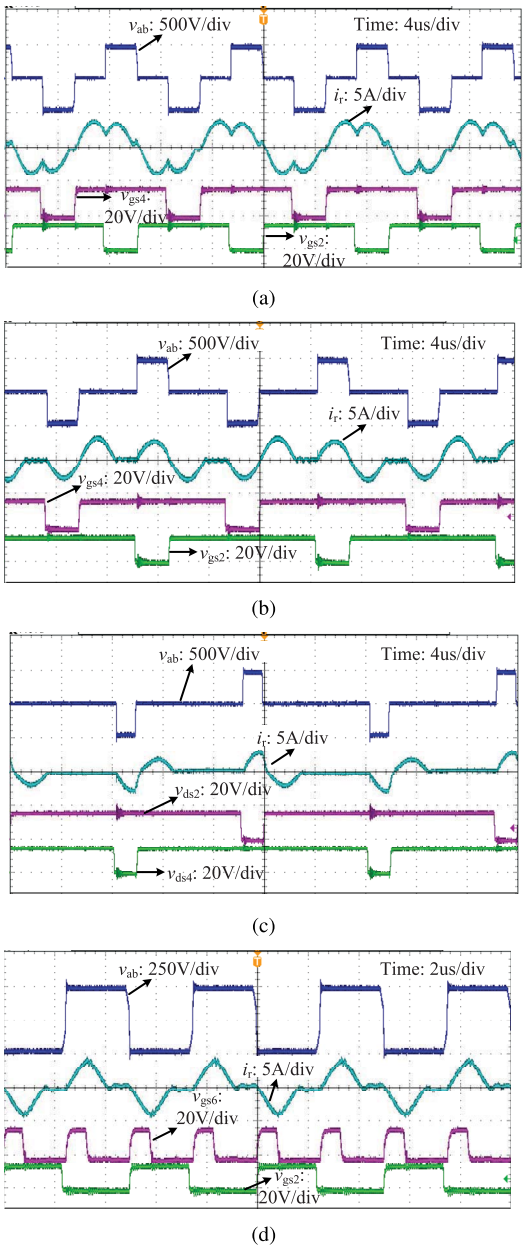


Fig. 14. Operation waveforms for transferring power from V_1 side to V_2. (a) Mode 2 with $V_1 = 480$ V and $V_2 = 24$ V. (b) Mode 3 with $V_1 = 480$ V and $V_2 = 24$ V. (c) Mode 4 with $V_1 = 480$ V and $V_2 = 24$ V. (d) Mode 1 with $V_1 = 240$ V and $V_2 = 56$ V.

at rectification mode, realizing ZCS-ON and OFF. In Mode 3, f_s is about 71 kHz below half of the resonant frequency. As shown in Fig. 14(b), all the switches turn ON/OFF when $i_r = 0$, thus realizing ZCS-ON/OFF. In Mode 4, f_s is fixed to

50 kHz, and D_p is controlled to regulate the power. As shown in Fig. 14(c), S_2 and S_4 realize ZVS-ON and ZCS-OFF. S_1 and S_3 are complements of S_2 and S_4, thus realizing ZCS-ON but suffering from hard turn-off.

For Mode 1, the normalized gain M is 1.87 with the input voltage being 240 V and the output voltage being 56 V. As shown in Fig. 14(d), f_s is 200 kHz, and D_s is regulated to control the power. S_1 and S_3 are complements of S_2 and S_4, S_2 is synchronous with S_3. The switches S_1–S_4 are controlled in complementary at duty 50% and turn ON/OFF with zero current. Output full-bridge operates at rectification mode. S_6 and S_8 are ZCS-ON.

In summary, 14 of the total 16 switching actions are soft-switching in Modes 1, 2, and 4, while all switching actions are soft switching in Mode 3. The reduction of the number of hard switching actions can help to reduce the switching losses, which will be verified in Section V-D.

In the reverse mode, the waveforms are similar to those of the forward mode, as shown in Fig. 15. The switching patterns, operating waveforms, and features of the switching actions are consistent with the analysis in Section II.

B. Mode Transition Waveforms

Fig. 16(a) shows the transition from Mode 4 (buck mode with low power level) to Mode 3 (buck mode with medium power level). The input voltage is 400 V, and the output voltage is regulated to 40 V. At the beginning, the load resistor is 7.5 Ω. The turning ON time is set to 1.69 μs, the converter works in Mode 4. Then the load is changed to 5 Ω, Mode 4 is switched to Mode 3, and the turning ON time rises from 1.69 to 2.32 μs, then the switching frequency is regulated from 50 to 55 kHz. Similarly, the transition from Mode 3 to Mode 4 is given in Fig. 16(b) with the same condition. The load is changed from 7.5 to 5 Ω. The operation mode can be seamlessly switched between Mode 4 and Mode 3.

Fig. 16(c) shows the transition from Mode 3 to Mode 2 (buck mode with high power level). The input voltage is 400 V, and the output voltage is regulated to 40 V. At the beginning, the load resistor is 4 Ω. The turning ON time is set to 2.32 μs, the converter works in Mode 3. Then the load is changed to 2.5 Ω, Mode 3 is switched to Mode 2, and the switching frequency is regulated from 66 to 110 kHz. Then Fig. 16(d) shows the transition from Mode 2 to Mode 3 under the same condition. The load is changed from 4 to 2.5 Ω. The transition waveforms verify that the operation mode can be seamlessly switched between Mode 3 and Mode 2.

Fig. 16(e) shows the transition between Mode 2 and 1 (boost mode). Because the boundary between buck and boost modes is the voltage gain $M = 1$. Thus the output voltage must be changed to realize the transition between buck and boost mode. The input voltage is 400 V, the output load is 5 Ω. In the beginning, the output voltage is 48 V and the converter works in Mode 2. Then Mode 2 is switched to Mode 1, and thus the switching frequency continues to rise from 126 to 200 kHz, then the conduction time D_sT_s of S_8 is continuously increased from 0 to 0.348 μs, until the output reaches a steady state. Similarly, the transition from Mode 1 to Mode 2 is given in Fig. 16(f) with the same condition. The output voltage is regulated from 56 to 48 V, showing the operation mode can be seamlessly switched between Mode 2 and Mode 1.

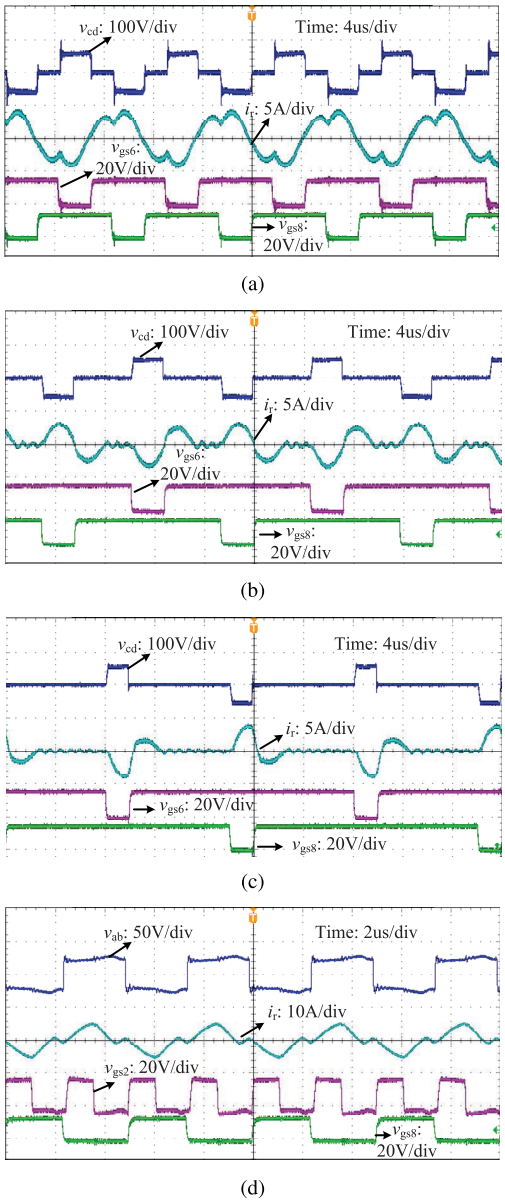


Fig. 15. Operation waveforms for transferring power from V_2 side to V_1. (a) Mode 6 with $V_2 = 56$ V and $V_1 = 240$ V. (b) Mode 7 with $V_2 = 56$ V and $V_1 = 240$ V. (c) Mode 8 with $V_2 = 56$ V and $V_1 = 240$ V. (d) Mode 5 with $V_2 = 24$ V and $V_1 = 480$ V.

Fig. 16(g) shows the transition between Mode 1 and 8 (buck mode with low power level for reverse power). The input voltage is 400 V, and the output voltage is controlled to be 56 V. In the beginning, the output load current is 10 A and the converter works in Mode 1. Then the output load is reversed to be −4 A. The the conduction time D_sT_s of S_8 is continuously decreased from 0.404 μs to 0. Then the converter works into Mode 8 and the switching frequency is switched to 50 kHz. Similarly, the transition from Mode 8 to Mode 1 is given in Fig. 16(h) with the same condition. The output load current is changed from −4 to 10 A. The operation mode can be seamlessly switched between Mode 1 and Mode 8.

Seamless transitions among different working modes can be achieved. Moreover, the computation time is only 5 μs

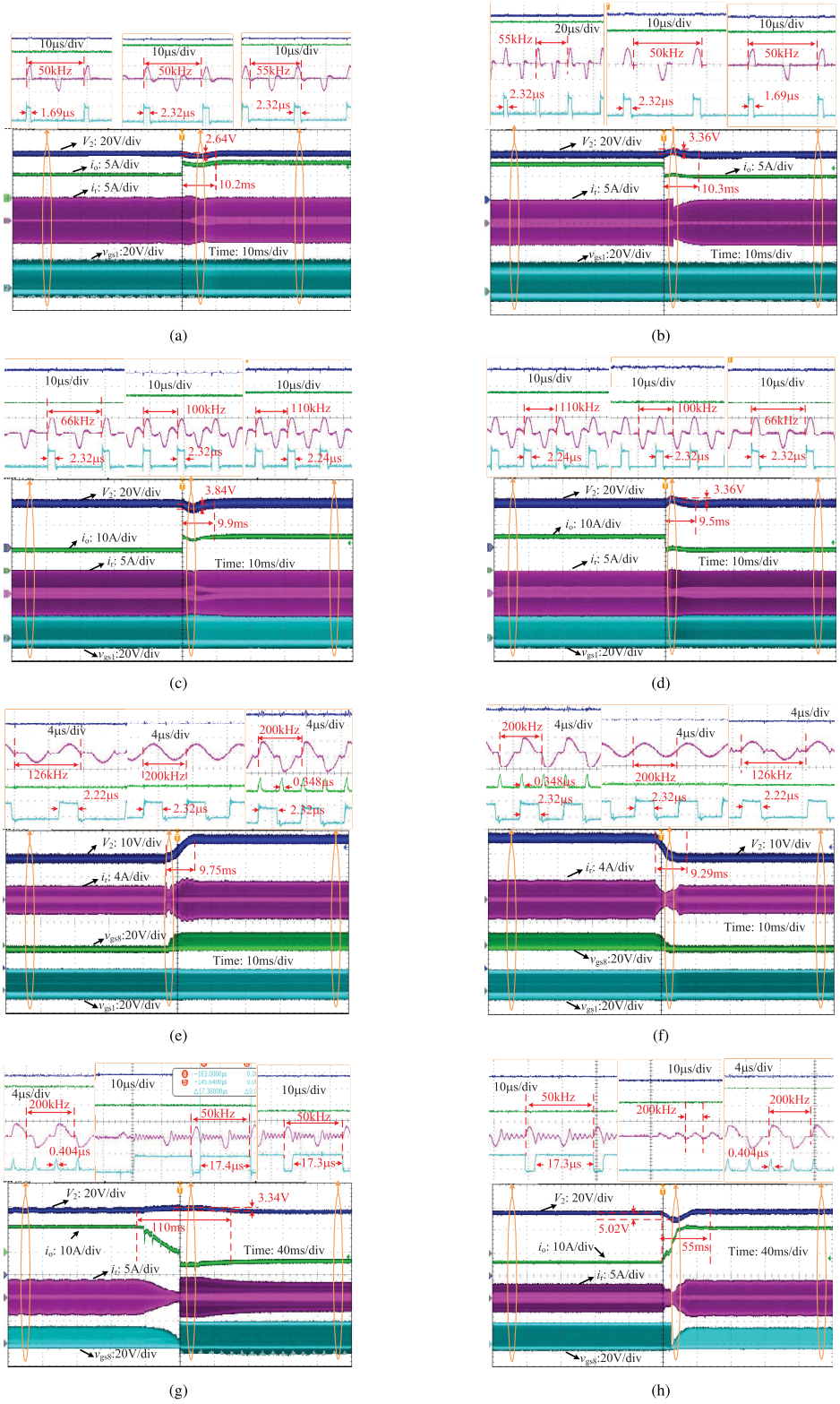
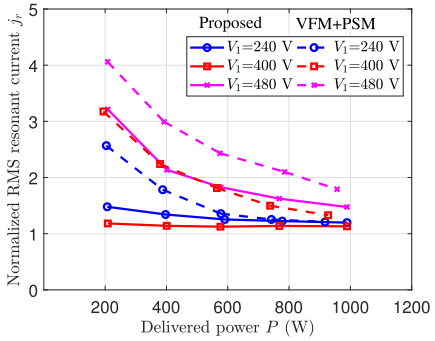


Fig. 16. Transitions waveforms between different work modes. Transition from (a) Mode 4 to 3, (b) Mode 3 to 4, (c) Mode 3 to 2, (d) Mode 2 to 3, (e) Mode 2 to 1, (f) Mode 1 to 2, (g) Mode 1 to 8, and (h) Mode 8 to 1.

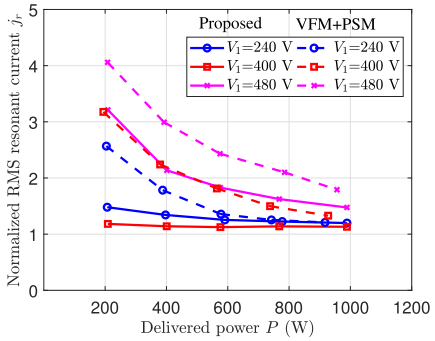
to update the switching sequence. The settling time is about 10 ms, which is acceptable compared with other papers.

C. Measured Circulation Current

With the direct measurement of the input current I_1 and the rms value of i_r, the normalized rms resonant current can be obtained through the calculation with (22). Fig. 17 shows the measured rms resonant current $j_{r,\mathrm{rms}}$ for the proposed modulation and the conventional VFM + PSM, under different input and output settings. Solid curves represent $j_{r,\mathrm{rms}}$ for the proposed modulation, while dashed curves represent that for the VFM + PSM. In Fig. 17(a), the BSRC is in the forward

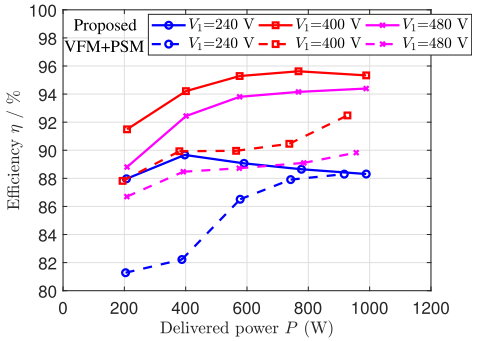


(a)

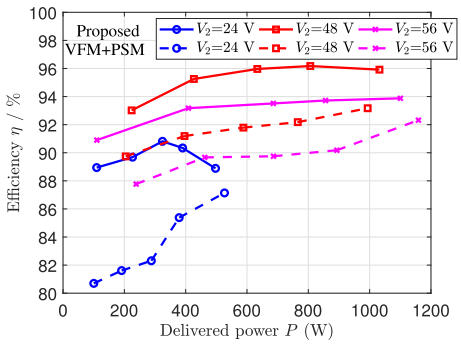


(b)

Fig. 17. Measured normalized rms resonant current versus output power. (a) Forward mode with $V_2 = 48$ V. (b) Reverse mode with $V_1 = 400$ V.



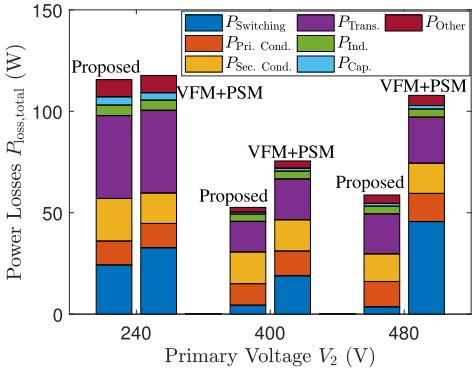
(a)



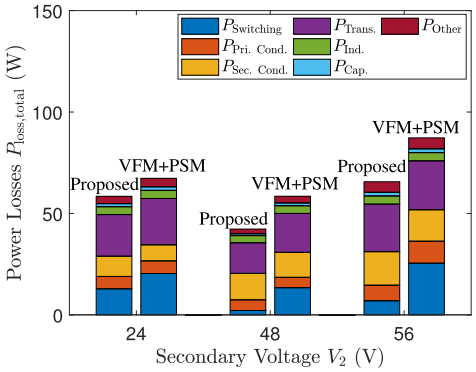
(b)

Fig. 18. Measured efficiency versus power. (a) Forward mode with $V_2 = 48$ V. (b) Reverse mode with $V_1 = 400$ V.

mode. The input voltage V_1 is set at 240, 400, and 480 V, while the output voltage V_2 is set at 48 V. The measured $j_{r,\mathrm{rms}}$ for the proposed modulation is smaller compared with



(a)



(b)

Fig. 19. Loss breakdown of BSRC with different modulations. (a) Forward mode with $V_2 = 48V$ and $I_2 = 20A$. (b) Reverse mode with $V_1 = 400V$ and $I_2 = 20A$.

that for the VFM + PSM. A similar observation can be obtained when the BSRC is in the reverse mode, as shown in Fig. 17(b). It verifies that the elimination of backflow power by the proposed modulation can reduce the rms value of the resonant current.

D. Measured Efficiency

The measured DC–DC efficiency of the BSRC is shown in Fig. 18. Solid curves represent efficiency for the proposed modulation, while dashed curves represent that for the VFM + PSM. It can be observed from Fig. 18(a) that, with the proposed modulation, the BSRC has better efficiency performance, especially under light load conditions. A similar observation can be obtained when the BSRC is in the reverse mode, as shown in Fig. 18(b). We can also observe that the efficiency in Mode 1 is lower than that in the other modes due to the higher switching frequency, the larger the resonant current, the lower the delivered power. In particular, normalized values rather than real values are used in Fig. 17. In consideration of the based of the normalized current shown in (22), although the normalized value in the pink case is higher than that in the blue case, the real value in pink case is smaller than that in the blue case. Thus, its efficiency could be higher.

Fig. 19 shows the traditional loss breakdown of the BSRC with the proposed modulation and the VFM + PSM. Due to

the elimination of backflow power and reduction of the hard switching actions, the switch and transformer losses for the proposed modulation are smaller than that for the VFM + PSM under different operating settings, which mainly contributes to the efficiency improvement for the proposed modulation.

VI. Conclusion

Backflow power is eliminated and switching loss is alleviated for a BSRC with a novel modulation scheme proposed in this article. The proposed modulation is formed by inserting zero voltage level and tuning the operating frequency along with the variation of the gain and the power level. The BSRC can operate in both buck- and boost-like modes for a wide gain range. Moreover, the resonant current can be fully released before the completion of the switching cycle to alleviate the hard turn-off problem. The number of hard switching actions is significantly reduced compared with existing modulation schemes in the literature. The proposed modulation is experimentally validated by a 1 kVA prototype of BSRC.

Appendix

The state equations have been given in Section II. In this section, we will discuss the constraint conditions of each working mode to calculate the initial values of the given state equations.

1) Mode 1: The operation during half switching cycle can be divided into three stages. Since the resonant current j_r and voltage m_r are continuous and the operations are symmetrical for positive and negative half cycles, the boundary conditions can be given as follow:

$$j_{r1} = (1 - m_{r0})\sin\varphi_1 \tag{A.1}$$

$$m_{r1} = (-1 + m_{r0})\cos\varphi_1 + 1 \tag{A.2}$$

$$0 = (1 - m_{r0} - M)\sin(\varphi_2 - \varphi_1) + j_{r1}\cos(\varphi_2 - \varphi_1) \tag{A.3}$$

$$-m_{r0} = (-1 + m_{r0} + M)\cos(\varphi_2 - \varphi_1) + j_{r1}\sin(\varphi_2 - \varphi_1) + 1 - M. \tag{A.4}$$

Moreover, the delivered current J_o is calculated as follows:

$$J_o = \frac{1}{\pi}\int_{\varphi_1}^{\varphi_2} j_r d\varphi. \tag{A.5}$$

The uncertainties in state equations can be achieved with (A.1)–(A.5) for a given D_s or P.

2) Mode 2: There are 2 stages during half switching cycle. The boundary conditions can be given as follow:

$$0 = (1 - m_{r0} - M)\sin\varphi_1 + j_{r0}\cos\varphi_1 \tag{A.6}$$

$$m_{r1} = (-1 + m_{r0} + M)\cos\varphi_1 + j_{r0}\sin\varphi_1 + 1 - M \tag{A.7}$$

$$-j_{r0} = (M - m_{r1})\sin(\varphi_2 - \varphi_1) \tag{A.8}$$

$$-m_{r0} = (m_{r1} - M)\cos(\varphi_2 - \varphi_1) + M. \tag{A.9}$$

Moreover, φ_2 is $\pi(f_r/f_s)$, which is decided by the delivered current J_o from the following equation:

$$J_o = \frac{1}{\varphi_2}\left(\int_0^{\varphi_1} j_r d\varphi - \int_{\varphi_1}^{\varphi_2} j_r d\varphi\right). \tag{A.10}$$

Then the variables can be derived as follow:

$$\varphi_1 = \arcsin\left[(2M - 1)\sin\frac{\varphi_2}{2}\right] + \frac{\varphi_2}{2} \tag{A.11}$$

$$j_{r0} = -\frac{\sin\varphi_1\sin(\varphi_2 - \varphi_1)}{\sin\varphi_2} \tag{A.12}$$

$$m_{r1} = -\frac{\sin(\varphi_2 - \varphi_1)}{\sin\varphi_2} + 1 - M \tag{A.13}$$

$$m_{r0} = -\frac{\cos\varphi_1\sin(\varphi_2 - \varphi_1)}{\sin\varphi_2} + 1 - M. \tag{A.14}$$

The duty cycle D_p is up to f_s

$$D_p = g(f_s) = \varphi_1\frac{f_s}{2\pi f_r} \tag{A.15}$$

$$\varphi_1 = \frac{\varphi_2}{2} + \arcsin[(2M - 1)\sin\varphi_2/2], \quad \varphi_2 = \pi\frac{f_r}{f_s}. \tag{A.16}$$

3) Mode 3: The BSRC works for a half resonant cycle during stage 1 and stage 3. Then the constraint conditions are

$$m_{r1} = 2 - 2M - m_{r0}, \tag{A.17}$$

$$-m_{r0} = 2M - m_{r1}. \tag{A.18}$$

Thus the values can be derived as follow:

$$m_{r1} = 1, \quad m_{r0} = 1 - 2M. \tag{A.19}$$

Moreover, the duty cycle D_p is calculated from $\varphi_1 = \pi$

$$D_p = \frac{f_s}{2f_r}. \tag{A.20}$$

4) Mode 4: There are 4 stages for half switching cycle, the conditions are as follows:

$$j_{r1} = (1 - m_{r0} - M)\sin\varphi_1 \tag{A.21}$$

$$m_{r1} = (-1 + m_{r0} + M)\cos\varphi_1 + 1 - M \tag{A.22}$$

$$(M + m_{r1})\sin(\varphi_2 - \varphi_1) = j_{r1}\cos(\varphi_2 - \varphi_1) \tag{A.23}$$

$$m_{r2} = (m_{r1} + M)\cos(\varphi_2 - \varphi_1) + j_{r1}\sin(\varphi_2 - \varphi_1) - M \tag{A.24}$$

$$\varphi_3 = \varphi_2 + \pi \tag{A.25}$$

$$-m_{r0} = 2M - m_{r2}. \tag{A.26}$$

The delivered current J_o is calculated as follows:

$$J_o = \frac{1}{\varphi_4}\left(\int_0^{\varphi_2} j_r d\varphi - \int_{\varphi_2}^{\varphi_3} j_r d\varphi\right). \tag{A.27}$$

With the help of MATLAB, the state variables at each working mode for a given condition can be achieved.

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