Onboard Energy Storage System Based on Interleaved High-Conversion-Ratio Quasi-Resonant Converter With Small Characteristic Impedance

Zhijian Fang, *Member, IEEE*, Zhiguo Wei, Zhicong Huang, *Member, IEEE*, and Fei Liu, *Senior Member, IEEE*

***Abstract*—An onboard energy storage system (OESS) withfast-energy-exchange capability is needed to enable future grid-to-vehicle (G2V) and vehicle-to-grid (V2G) operations. To facilitate the fast energy exchange, the OESS normally interfaces between a high voltage (HV) bus on the grid side and a low voltage (LV) bus on the vehicle side. The HV bus can be up to 1200 V, while the LV bus is as low as 48 V, which means a high conversion ratio is needed. Resonant converters are commonly used for OESS and designed with large characteristic impedance for wide-range output power and zero-voltage-switching operation. However, such a design leads to large volume and complex customization of the magnetic components. In this paper, a high-conversion-ratio OESS is proposed, which is based on interleaved quasi-resonant converters with small characteristic impedance. The resonant converters are of modular design with a small characteristic impedance to achieve small volume, low cost, and simple customization. Interleaved in LV-side-parallel and HV-side-series configuration, a high conversion ratio can be achieved. Moreover, modulated in quasi-resonant operations, all the switches can realize soft switching even at light load conditions for high efficiency. Burst control for output regulation is implemented in each modular quasi-resonant converter, while interleaved control is implemented between them to minimize the current ripple. The proposed design and control are validated by a compact 5 kW prototype with a charging/discharging current of 100 A, high power efficiency of 98.91%, a high power density of 3.86 W/cm^3, and high-conversion-ratio (up to 20: 1) power flow between a 1000 VDC HV bus and a 48 VDC LV bus.**

***Index Terms*—Onboard energy storage system, resonant converter, small characteristic impedance, zero current switching, high conversion ratio.**

I. Introduction

ELECTRIC vehicle (EV) is being an important part of next-generation smart grid [1]–[3]. Rather than unidirectionally acquiring energy from the grid to power the motors, the future EV should allow storing excess renewable generation and feeding electricity back in the periods of high power demand. Therefore, a bidirectional onboard energy storage system (OESS) is needed to enable grid-to-vehicle (G2V) and vehicle-to-grid (V2G) operations [4]. The OESS acts as an interface between a high-voltage (HV) bus on the grid side and a low-voltage (LV) bus on the battery side. The HV bus is usually converted from the AC power grid leveled at 380 VAC, 220 VAC or 110 VAC, which means the HV bus ranges from 400 to 800 VDC [5], [6]. Recently, due to the requirements of high-power transfer for extreme fast energy exchange, the voltage level of the HV bus will be further increased up to 1000 VDC [7]. On the contrary, the voltage level of the LV bus is determined by the requirement of the electric drive onboard, which is much lower than that of the HV bus. Nowadays, the required voltage level of the electric drive ranges from 200 to 400 VDC [8], [9], but 48 VDC electrified drivetrain technology for future hybrid and electric vehicles are being developed [10]–[12]. Moreover, from the perspectives of battery management issues and safety concerns, it is preferred to construct the battery pack by cascading the battery cells in parallel connection rather than series connection. For the above two reasons, the LV bus at the battery side is considered as low as 48 VDC in this paper. Therefore, a high conversion ratio is required for the OESS.

Dual active bridge (DAB) converter has been widely studied and used as the OESS, due to simple symmetric structure, bidirectional power transfer capability, and small numbers of passive components [13], [14]. It is usually difficult for the DAB converter to maintain zero voltage switching (ZVS) for high efficiency especially in light load conditions [15]–[17]. Critical conditions to achieve ZVS are analyzed in [15], which are commonly influenced by the junction capacitance and the resonant inductance. The guidelines of the inductor design for ZVS range are given in [6], [18], [19]. Although larger inductance can ensure a wider ZVS operation range, cost and volume will increase as penalties. Alternatively, various modulation methods are proposed to extend the ZVS operation range, such as extending phase shift modulation, dual phase shift modulation, triple phase shift modulation *et al.* [10], [20]–[24]. However, these modulations are too complex and will even cause a large reactive current, which lowers the converter efficiency and thus requires a large-volume heat sink. As illustrated in [25], the reactive power can be minimized by using large inductance, but

Manuscript received April 14, 2020; revised September 7, 2020 and February 6, 2021; accepted April 4, 2021. Date of publication April 7, 2021; date of current version June 9, 2021. This work was supported by the National Natural Science Foundation of China under Grants 51707138 and 52007067. The review of this article was coordinated by Prof. C.M. Lai. *(Corresponding author: Zhicong Huang.)*

Zhijian Fang and Zhiguo Wei are with the School of Automation, China University of Geosciences (Wuhan), Wuhan 430074, China, and also with the Hubei Key Laboratory of Advanced Control and Intelligent Automation for Complex Systems, Wuhan 430074, China (e-mail: fangjianhust@gmail.com; wzg1378941@163.com).

Zhicong Huang is with the Shien-Ming Wu School of Intelligent Engineering, South China University of Technology, Guangzhou 510006, China (e-mail: zhiconghuang@scut.edu.cn).

Fei Liu is with the School of Electrical Engineering, Wuhan University, Wuhan 430072, China (e-mail: lf_dyj@whu.edu.cn).

Digital Object Identifier 10.1109/TVT.2021.3071525

leading to a heavy inductor in return. Moreover, the resolution of phase shift modulation is usually restricted by the PWM generation unit of the microcontrollers, such that the switching frequency of the DAB converters are usually as low as 20 kHz, leading to large transformer and resonant inductance [22].

Compared with the DAB converters, the resonant converters can operate at a higher operating frequency, resulting in a smaller volume of the transformer and resonant inductance. Among the resonant converters, a widely studied and used CLLC resonant bidirectional converter features ZVS for input bridge and zero current switching (ZCS) for output bridge [26]–[29]. The switching frequency can be up to 1 MHz by using variable frequency modulations [30], [31]. However, the gain range of the converter is decided by the resonant tank limiting the operating range. To extend the operation range, the ratio of the resonant inductance to the magnetic inductance should be high enough, which will increase the volume and power losses. A pulse width modulation (PWM) is proposed for series resonant DC/DC converter with full bridge on the primary side and half bridge on the secondary side [32]. The duty cycle is regulated to control the power with a fixed switching frequency. Large inductances are needed to reduce the reactive current. Nevertheless, a large resonant inductor is needed in the above literature to achieve a wide gain range and small reactive current.

In the above studies of OESS based on DAB converters and resonant converters, a large inductor is commonly required to extend the ZVS region, widen the gain range and reduce the reactive current at the expense of increasing the converter's volume and cost. PCB planar inductor is used to reduce the cost and volume in [31], [33]. The magnetic field distribution is calculated by using the computer to guide the inductor design, making this design methodology complex in practical implementation. Ref. [34], [35] propose to integrate the inductor and the transformer to reduce the cost and magnetic volume. However, it makes transformer customization and production difficult in practice. Moreover, the power losses of the transformer will be increased, leading to a large-volume thermal design. For the above reasons, the separated inductors are still commonly used in most OESS applications, which are not compact designs.

This paper aims to design an OESS that features a) high power density, b) high power efficiency and c) high conversion ratio. To achieve all these objectives, this paper proposes an OESS based on the interleaved high-conversion-ratio quasi-resonant converter with a small characteristic impedance. Three features are achieved in the proposed converter: (a) high power density for small characteristic impedance and small inductor is used in the quasi-resonant converter, which can also be integrated into the transformer, reducing the volume and the cost; (b) fully soft switching because the converters are modulated in a quasi-resonant operation, the resonant current is discontinuous and all the switches can realize ZCS ON and OFF (ON/OFF) even at the light load conditions; (c) simple control method, burst control for output regulation is implemented in each quasi-resonant converter and self voltage and current sharing are realized without complex balance method due to LV-side-parallel and HV-side-series configuration, which also achieves a high conversion ratio. With the above design and control, a compact 5 kW prototype of OESS with a charging/discharging current of 100 A is implemented, achieving high efficiency of 98.91%, a high power density of 3.86 W/cm^3, and a high-conversion-ratio (up to 20: 1) power flow between a 1000 VDC HV bus and a 48 VDC LV bus.

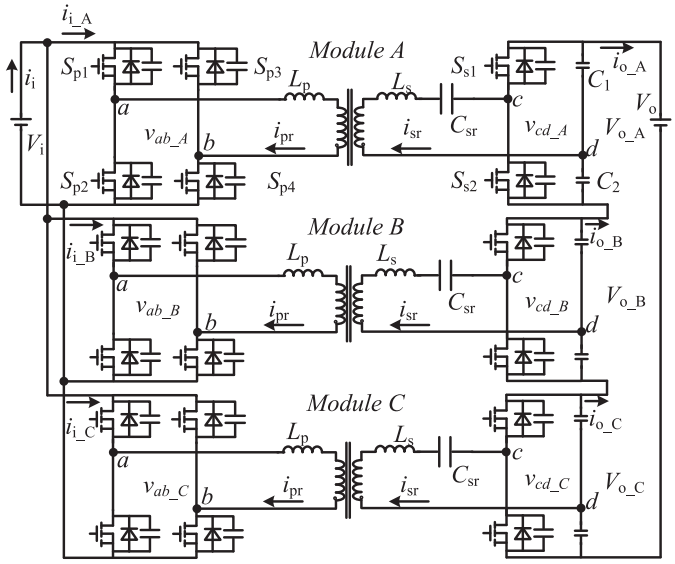

Fig. 1. Overall structure of the proposed OESS.

II. System Structure

A. Interleaved Configuration

Fig. 1 shows the proposed OESS, which is based on a three-phase interleaved quasi-resonant converter with a small characteristic impedance. The proposed system interfaces between the LV bus at the battery side leveled at about 48 V 60 V and the HV bus at the grid side ranging from 1000 V to 1200 V. To meet the required conversion ratio around 20: 1, a modular design is adopted and the proposed system consists of three modular quasi-resonant converters. On the LV bus side, the quasi-resonant converters are in parallel connection to share large current, while on the HV bus side, they are in series connection as a voltage divider. Such that, the required voltage gain of each module can be reduced to 1: 7 approximately, which makes the transformer design easy. Moreover, complex control for current sharing and voltage balancing can be implemented with such an interleaved configuration.

B. Resonant Converter With Small Characteristic Impedance

Fig. 2 shows the schematics of the modular converter, which is a quasi-resonant converter with a small characteristic impedance. The voltage gain of the quasi-resonant converter is about 7. A full bridge inverter is connected to the LV bus and generates a high-frequency AC voltage v_{ab} to drive a high frequency transformer. On the HV bus side, a half bridge converter rectifies the AC voltage v_{cd} into DC voltage V_{o_m}. m represents the number of the modular converter and can be A, B and C. L_p, and L_s are the leakage inductances of the transformer on the LV

TABLE I
COMPARISON OF THE CHARACTERISTIC IMPEDANCE

Topology	Bi-LLC [26]	CLLC [27]	CLLC [29]	CLLC [32]	DAB [36]	Proposed
LV bus voltage (V)	24 – 48	380	250 – 420	400 (for half bridge)	11.2 – 14.4	48 – 60
HV bus voltage (V)	200 – 400	380	400 – 550	250 – 415	360 – 420	1000 – 1200
Power (W)	500	5000	3300	3300	1000	5000
Frequency (kHz)	65 – 165	55 – 75	100 – 130	50	100	100
Resonant inductance (μH)	76	30	31.69	22.56 (14.89 at LV side)	26	8
Resonant capacitance (nF)	15.37	200	53.18	396 (600 at LV side)	-	220
Characteristic impedance (Ω)	70.314	12.25	24.411	7.55	16.33	6.03
Quality factor	1.57	0.523	3.58	0.507	1	0.383

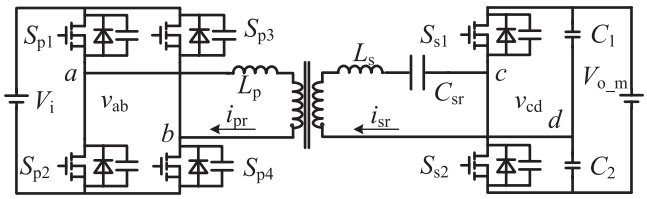

Fig. 2. Schematics of the modular quasi-resonant converter with small characteristic impedance.

bus side and HV bus side, respectively. A resonant capacitor C_{sr} is used to compensate the leakage inductance of the transformer. C_1 and C_2 are the DC filter capacitors. It should be noted that, due to modular design, the parameters of the modular converters are identical to each other.

The schematic of the modular converter enables bidirectional operation. When the battery is discharged, the full bridge converter is enabled to converter the DC voltage to the high frequency AC voltage, while the half bridge converter is disabled or synchronous rectifying operation, working as a diodes rectifier to convert the AC voltage to the DC voltage. When the battery is charged, the full bridge converter is disabled while the half bridge is enabled to convert the power.

The resonant tank is decided by the resonant frequency and the characteristic impedance. The resonant frequency is usually determined by the switching frequency range, which is relevant to the volume design of the transformer and the inductor. The characteristic impedance has a significant influence on the gain feature of the converter, defined as

$$Z_r = \sqrt{\frac{L_r}{C_r}}, \tag{1}$$

where L_r and C_r are the resonant inductance and capacitance of the converter, given by

$$C_r = C_{sr}, \text{and} \tag{2}$$

$$L_r = L_p n^2 + L_s, \tag{3}$$

respectively. n is the transformer ratio. L_p and L_r are the leakage inductances of the primary and secondary sides of the transformer, respectively. For the conventional bidirectional resonant converters, large characteristic impedance Z_r achieves cliff gain curve for wide voltage gain range, but results in large inductor volume and high power losses as discussed in Section I. Unlike the conventional design, the proposed resonant converter is designed with a small characteristic impedance. With the utilization of the small interior leakage inductance of the transformer, a customized design of the transformer for large leakage inductance and small magnetizing inductance is not required. Moreover, there is no air gap in the high frequency transformer magnetic core, and small power loss of the transformer can be achieved. Table I summarizes the key parameters of several converters in literature. All the resonant inductors and capacitors reflected on the HV bus side are highlighted. It should be noted that in [32], the LV side of the converter is half bridge structure and resonant capacitors are integrated into the capacitances of the half bridge. Thus the equal resonant capacitance on LV side is 0.6 μH and the equal LV voltage is 200 V. It can be observed that the proposed resonant converter in this paper has a very small characteristic impedance. Since the resonant frequency and power are different in published papers, the quality factors are calculated for the comparison among these converters. The resonant converter in this paper has the smallest quality factor and characteristic impedance.

III. QUASI-RESONANT MODULATION FOR ZCS ON/OFF

The key waveforms of the proposed quasi resonant converter are shown in Fig. 3. The operation mechanism of the converter at the positive half period is similar to the one at the negative half period. Therefore, only the operation mechanism at the positive half period is analyzed in this section. Before the discussion, some assumptions are given to simplify the analysis as follows.

1) All the switches are ideal without power loss.
2) All the elements are ideal without power loss.
3) The transformer is nearly ideal with a very small leakage inductance and a very large magnetic inductance.
4) The input and output capacitors are large enough to maintain constant voltage buses.

The modulation of the quasi-resonant converter for ZCS can be divided into four modes as follows.

Mode 1 (t_0 to t_1): In this mode, the switches S_{p1} and S_{p4} are turned ON. The primary resonant current i_{pr} flows through V_i, S_{p1}, the transformer T_r as well as S_{p4}. The secondary resonant current i_{sr} flows through T_r, the resonant capacitor C_r as well as the junction capacitors of S_{s1} and S_{s2}, as shown in Fig. 4(a). i_{sr} increases from zero to charge the equivalent switch junction capacitances C_{sj} as shown in Fig. 4(a). i_{sr} is given by

$$i_{sr} = 2C_{sj}\frac{\mathrm{d}v_{cd}}{\mathrm{d}t}, \tag{4}$$

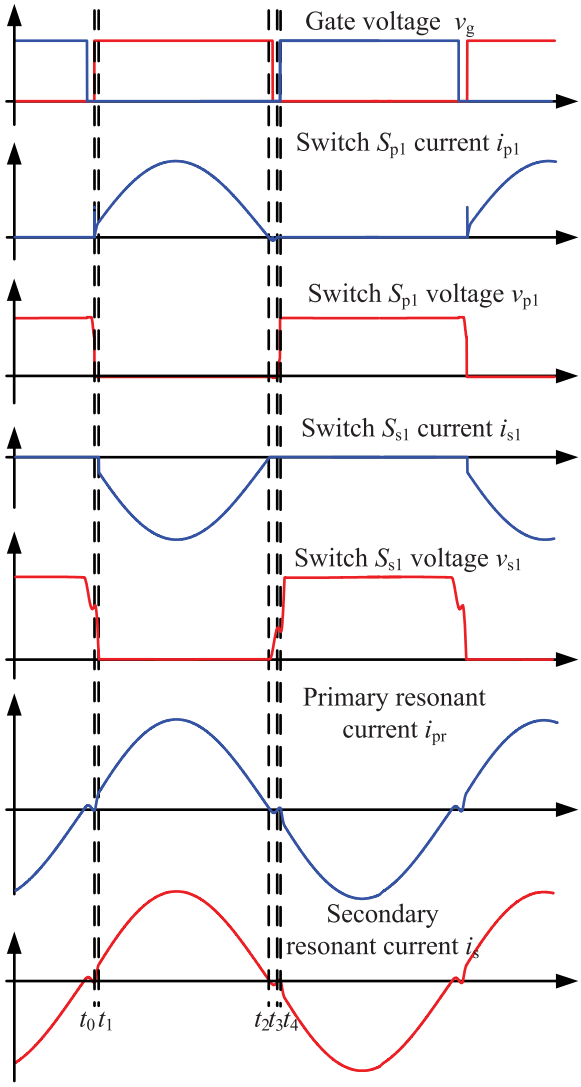

Fig. 3. Switching sequence for ZCS and key operating waveforms.

where C_{sj} is the junction capacitance of S_{s1} and S_{s2}, and v_{cd} is the terminal voltage of secondary bridges. Based on the equivalent circuit shown in Fig. 6(a), i_{sr} can be derived as

$$i_{sr} = (nV_i - v_{sr0} - v_{cd0})2\pi f_{rs} C_{r1} \sin(2\pi f_{rs} t). \quad (5)$$

v_{sr0} and v_{cd0} are the initial values of the C_r and C_{sj} voltages at t_0, respectively. C_{r1} is the total equivalent capacitance of C_r and C_{sj}, given by

$$C_{r1} = \frac{C_r C_{sj}}{C_r + C_{sj}}. \quad (6)$$

The equivalent circuit in Fig. 4(a) is resonant at a secondary resonant frequency f_{rs}, given by

$$f_{rs} = \frac{1}{2\pi\sqrt{L_r C_{r1}}}. \quad (7)$$

At t_0, the switches S_{p1} and S_{p4} are turned ON with zero current realizing ZCS. When v_{cd} increases from the initial voltage v_{cd0} to half of the output voltage, i.e., $\frac{V_{o\_m}}{2}$, the freewheeling diode of S_{s1} is conducted until Mode 2 begins.

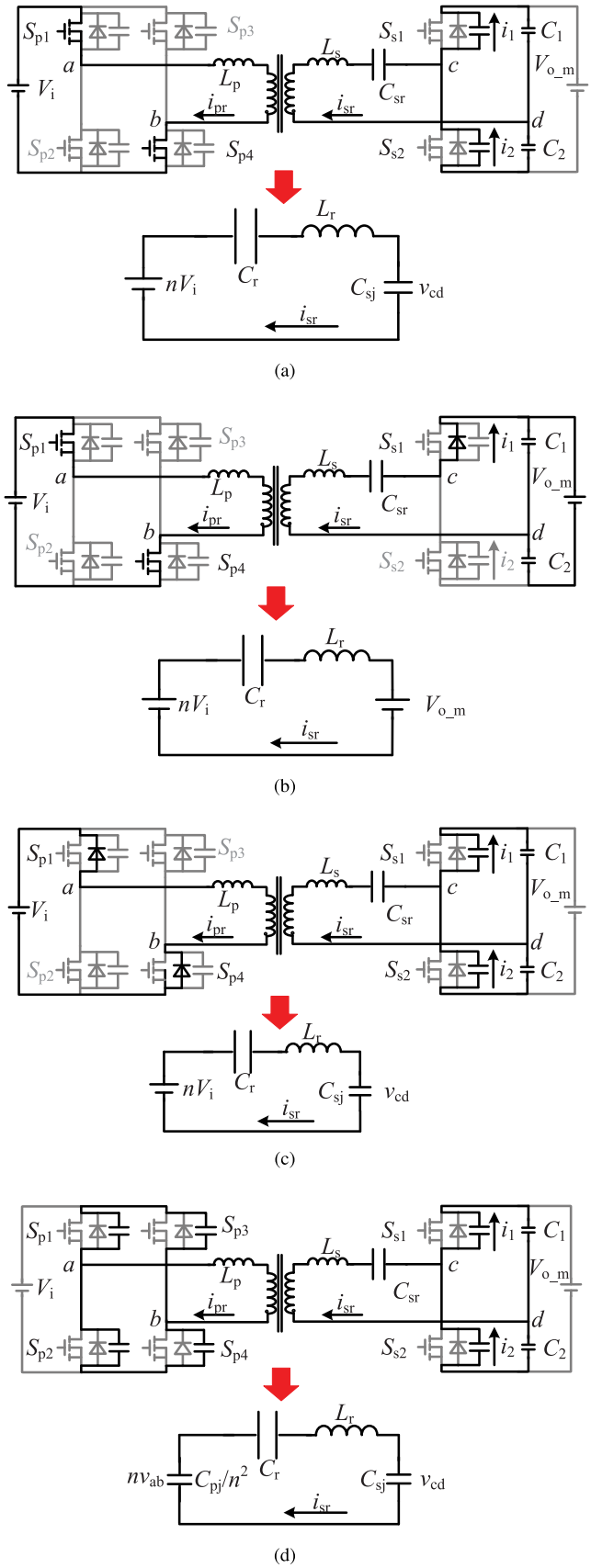

Fig. 4. Power flow and equivalent circuit model of the modular quasi-resonant converter.

Mode 2 (t_1 to t_2): When i_{sr} flows through the freewheeling diode, *Mode 2* begins as shown in Fig. 4(b). S_{s1} can be turned ON with an interval of time lagging t_1 and turned OFF with an interval of time leading t_2 to realize synchronous rectification achieving ZVS ON and ZCS OFF. As the equivalent circuit is shown in Fig. 4(b), the LV side bus is connected with the HV DC bus side via the L_r-C_r resonant tank. Power is delivered from the battery side to the HV DC bus side. i_{sr} could sinusoidally rise to the peak value and fall to zero at t_2. i_{sr} can be derived as

$$i_{sr} = (nV_i - V_{o\_m}/2 - v_{sr1})2\pi f_r C_r \sin(2\pi f_r(t - t_1)) + i_{sr1}\cos(2\pi f_r(t - t_1)), \quad (8)$$

where v_{sr1} and i_{sr1} are the resonant voltage and current values at t_1. f_r is the resonant frequency of C_r and L_r, given by

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \quad (9)$$

Mode 3 (t_2 to t_3): At this mode, i_{pr} flows through the anti-diodes of S_{p1} and S_{p4} to charge V_i, as shown in Fig. 4(c). Since the secondary switch S_{s1} is turned OFF, i_{sr} will charge the junction capacitors. Switches S_{p1} and S_{p4} can be turned OFF during this period realizing ZCS OFF, because i_{sr} flows through the anti-diodes of the switches. When i_{pr} reaches zero again, this mode ends. i_{sr} can be achieved from the equivalent circuit in Fig. 4(c).

$$i_{sr} = (nV_i - V_{o\_m}/2 - v_{sr2})2\pi f_{rs} C_{r1} \sin(2\pi f_{rs}(t - t_2)), \quad (10)$$

where v_{sr2} is the resonant voltage value at t_2. The equation is similar with (8). The current i_{sr} is negative at *Mode 3* while positive at *Mode 2*.

Mode 4 (t_3 to t_4): At this mode, all switches are turned OFF. The full bridge circuit on the LV bus side can be considered as a capacitor. All the components are free-oscillating, as shown in Fig. 4(d). Since most of the energy stored in the resonant tank has been absorbed by the voltage source, the resonant current i_{sr} is small during this period and will quickly be reduced to zero due to the inner resistors of resonant components and switches. Switches S_{p2} and S_{p3} can be turned ON at t_4 realizing ZCS-on. The resonant current can be calculated as follows ignoring the inner resistors.

$$i_{sr} = (nV_i - v_{sr3} - v_{cd3})2\pi f_{rt} C_{r2} \sin(2\pi f_{rt}(t - t_3)), \quad (11)$$

where v_{sr3} and v_{cd3} are the resonant voltage values of C_r and C_{sj}. C_{r2} is the total equal capacitors of the equivalent circuit in Fig. 4(d), given by

$$C_{r2} = \frac{C_r C_{sj} C_{pj}/n^2}{C_r C_{sj} + C_r C_{pj}/n^2 + C_{sj} C_{pj}/n^2}, \quad (12)$$

where C_{pj} is the junction capaitances of primary switches. f_{rt} is the third resonant frequency of L_r and C_{r2}, given by

$$f_{rt} = \frac{1}{2\pi\sqrt{L_r C_{r2}}}. \quad (13)$$

This mode ends up at the time of half cycle.

Designed with a quasi-resonant switching frequency, which is slightly smaller than the resonant frequency f_r, the primary switches can be turned OFF in *Mode 3* during t_2 to t_3, achieving a quasi-resonant switching frequency f_s, which is slightly smaller than the resonant frequency f_r. During this period, the resonant current can flow through the anti-diodes of the switches and thus the switches can realize ZCS OFF in *Mode 3*. The switches are designed to be ON in *Mode 4* by choosing the deadtime. Due to the design of small characteristic impedance, the energy stored in the resonant tank is very small. The resonant current should be quickly damped to zero by the inner resistors during t_3 to t_4. Such that, the primary switches can realize ZCS ON in *Mode 4*. Moreover, the secondary can achieve ZVS ON and ZCS OFF by using synchronous rectification. All the switches can realize ZCS ON and OFF, eliminating large turn-off losses compared with sole ZVS-ON modulations in conventional resonant converters with a large characteristic impedance. Therefore, a high power efficiency can be achieved due to the small switching losses.

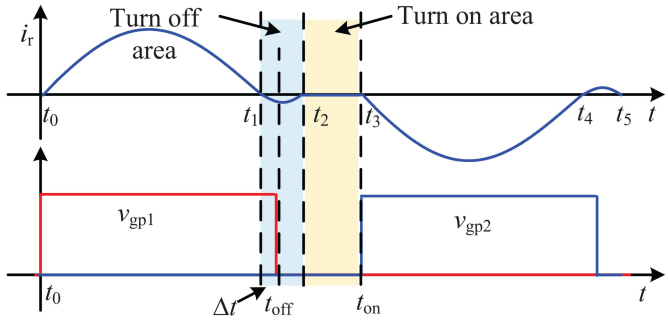

Fig. 5. Simplified steady-state waveforms of the quasi-resonant operation.

IV. Design Considerations for Small Characteristic Impedance

A. Switching Frequency and Dead Time

Based on the quasi-resonant operation analyzed in Section III, the operating waveforms of the converter shown in Fig. 3 can be simplified as Fig. 5. Operation in *Mode 1* and the free-oscillating in *Mode 4* can be ignored because the operating time is very short. Thus, t_1 is the half resonant period, $\frac{1}{2f_r}$, and t_2-t_1 is half of the secondary resonant period, $\frac{1}{2f_{rs}}$. The waveforms of the resonant current, as well as the switching sequence, are shown in Fig. 5. In order to achieve ZCS ON/OFF, the switches should be turned OFF during t_1 to t_2 and turned ON during t_2 to t_3.

During t_0 to t_1, the resonant current i_r is sinusoidal with resonant frequency f_r, as given in (9). During t_1 to t_2, the resonant current varies from zero to negative, resonating with the junction capacitance, resonant inductance and capacitance, because the switches S_{p1} and S_{p4} are still on. The current should resonate with L_r, C_r, and C_{sj} at the secondary resonant frequency f_{rs}, which has been defined as (7). With (7) and (9), the turn-off time t_{off} and the turn-on time t_{on} can be derived as

$$t_{off} = t_1 + \Delta t = \frac{1}{2f_r} + \Delta t, \text{and} \quad (14)$$

$$t_{on} = t_3 = \frac{1}{2f_s}, \quad (15)$$

where f_s is the switching frequency. The dead time is defined as

$$t_d = t_{on} - t_{off}. \tag{16}$$

To satisfy the requirement of ZCS ON/OFF, Δt can be determined and designed as

$$0 \le \Delta t \le t_2 - t_1 = \frac{1}{2f_{rs}}. \tag{17}$$

Therefore, the swiching frequency f_s and the dead time t_d can be designed as

$$f_s \le \frac{f_{rs} f_r}{f_{rs} + f_r}, and \tag{18}$$

$$\frac{1}{2f_s} - \frac{1}{2f_r} - \frac{1}{2f_{rs}} \le t_d \le \frac{1}{2f_s} - \frac{1}{2f_r}. \tag{19}$$

From (18) and (19), the ZCS operation range is only decided by the switching frequency and the dead time, which means it is independent of the load. Therefore, the suitable switching frequency can be fixed to realize soft switching over all load conditions, achieving high efficiency for the resonant converter with minimum control effort.

B. Resonant Capacitor

In order to achieve high power density and efficiency, a small characteristic impedance is designed in this paper. The small leakage inductance of the transformer is used as the resonant inductance. Therefore, the resonant capacitance can be derived from equations (9).

$$C_r = \frac{1}{(2\pi f_r)^2 L_r}. \tag{20}$$

The peak voltage value of resonant capacitor v_{peak} can be derived as

$$v_{peak} = i_{peak} \frac{1}{2\pi f_r C_r}, \tag{21}$$

where i_{peak} is the peak current value, which is derived as

$$i_{peak} = \frac{\pi f_r i_d}{2f_s}, \tag{22}$$

based on the current-balance principle. i_d is the HV DC bus current.

C. Transformer

The power loss of the transformer donates most to the total power loss of the converter and affects the design of weight and volume. In order to match the input and output voltages, the turn ratio should be designed as

$$n = \frac{V_o}{6V_i}. \tag{23}$$

Due to the high frequency, the ferrite core is chosen based on the converter rated power. Primary turn number of the transformer is derived as

$$N_p = \frac{V_i}{4f_s B A_e}, \tag{24}$$

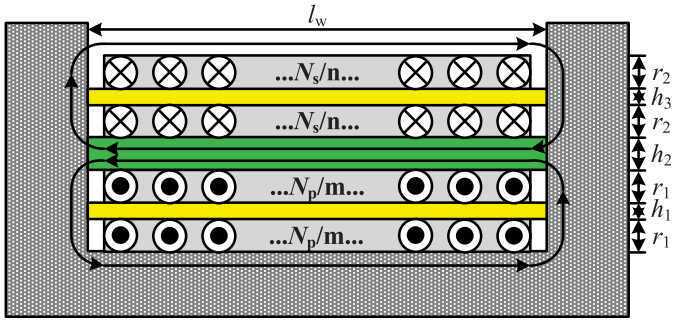

Fig. 6. Winding sequence of the transformer.

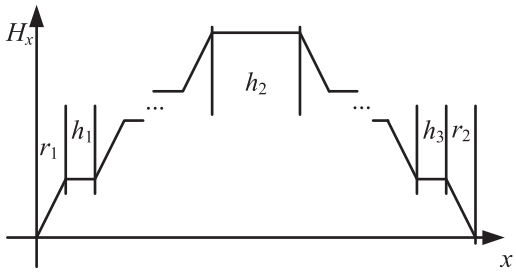

Fig. 7. Curve of magnetic field varying with the height.

where B is the rated magnetic flux density and A_e is the effective cross sectional area that can be obtained from the datasheet of the ferrite core. With the required turn ratio given in (23), the secondary turn number of the transformer is derived accordingly.

Based on the rated resonant current (22), the litz wire can be chosen. In order to integrate the resonant inductor into the transformer, the winding type should be designed carefully. All the primary windings are placed innermost on the bobbin. The minimum length of wire is achieved to reduce the conduction loss in the wire. The secondary windings are placed outmost on the bobbin to achieve high voltage. The winding sequence is shown in Fig. 6. The primary side has m layers while the secondary side has n layers. The diameter of primary and secondary wires are r_1 and r_2. h_1 is the turning space of the primary winding, h_3 is the turning space of the secondary winding and h_2 is the turning space between the primary and the secondary winding. l_w is the width of the window.

The magnetic field varying with the height is shown in Fig. 7. The magnetic field increases with the height rising and it will maintain constant during the air gap. Since the anti-currents of the secondary side winding, the magnetic field will reduce with the height rising during the secondary winding area. Thus, the leakage inductance of the transformer can be calculated as

$$L_{le} = \frac{\mu_0 N_p^2}{l_w} \left(l_{av2} h_2 + \frac{m r_1 l_{av1}}{3} + \frac{n r_2 l_{av3}}{3} + \frac{\sum_{i=1}^{m-1} i^2}{m^2} l_{av1} h_1 + \frac{\sum_{j=1}^{n-1} j^2}{n^2} l_{av3} h_3 \right), \tag{25}$$

where l_{av1}, l_{av2}, and l_{av3} are the average length of the primary, air gap, and secondary side winding.

D. Design Case

A design case is showcased in this section with the guidelines above. There are five critical design parameters: transformer turn ratio, number of windings, resonant inductor, resonant capacitor, and deadtime. The given conditions are input voltage $48\tilde{}V$ $60\tilde{}V$, output voltage $1000\tilde{}V$ $1200\tilde{}V$, resonant frequency 120 kHz, primary and secondary switches specifications. Assume the switching frequency is about 100 kHz, smaller than the resonant frequency. The design process is expressed as follows.

- *Step 1:* Calculate the turn ratio of the transformer. The input voltage is $48V$ $60V$ and the output voltage is $1000V$ $1200V$. Based on equation (23), the turn ratio is

$$n_{\min} = \frac{V_{o,min}}{6V_{i,min}} = \frac{1000V}{6 \times 48V} = 3.47. \tag{26}$$

  Thus turn ratio is chosen as $n = 3.75$.
- Step 2: Calculate the primary and secondary numbers of windings. From equation (24), the primary turns is

$$N_p = \frac{V_i}{4 f_s B A_e} \tag{27}$$

$$= \frac{60V}{4 \times 100\text{kHz} \times 200\text{mT} \times 225\text{mm}^2} = 3.333, \tag{28}$$

  where the core is ELP 43/10/28 with ELP 43/10/28. Then primary turns is 4 and secnodary turns is 15.
- Step 3: Achieve the resonant inductor value. The switching frequency is close to 100 kHz. The leakage inductance of the transformer can be measured at 100 kHz, which is about 8 μH. Then the resonant inductor is 8 μH.
- Step 4: Calculate the resonant capacitor. From equation (20), the resonant capacitor C_r can be achieved.

$$C_r = \frac{1}{(2\pi f_r)^2 L_r} \tag{29}$$

$$= \frac{1}{(2 \times \pi \times 120\text{kHz})^2 \times 8\mu\text{H}} = 0.22\mu F, \tag{30}$$

  where resonant frequency is set to 120 kHz.
- Step 5: Determine the switching frequency and the deadtime. The junction capacitor of secondary MOSFET is 0.91 nC. Then the secondary resonant frequency can be obtained from equation (7)

$$f_{rs} = \frac{1}{2\pi\sqrt{L_r C_{r1}}} \tag{31}$$

$$= \frac{1}{2 \times \pi \times \sqrt{8\mu\text{H} \times 3.64\text{nC}}} = 836.5\text{kHz}. \tag{32}$$

  The switching frequency can be decided by

$$f_s \le \frac{f_{rs} f_r}{f_{rs} + f_r} \tag{33}$$

$$= \frac{836.5\text{kHz} \times 120\text{kHz}}{836.5\text{kHz} + 120\text{kHz}} = 104.945\text{kHz}. \tag{34}$$

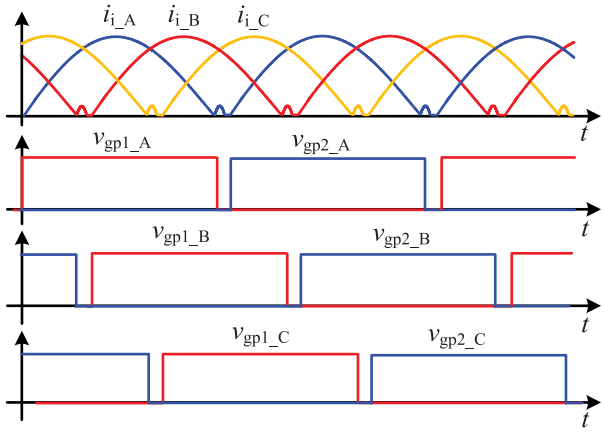

Fig. 8. Driving sequence for interleaved modulation and corresponding waveforms of the OESS.

The switching frequency is chosen to be 100 kHz. And the deadtime can be determined from equation (19),

$$\frac{1}{2 \times 100\text{kHz}} - \frac{1}{2 \times 120\text{kHz}} - \frac{1}{2 \times 836.5\text{kHz}} \tag{35}$$

$$= 235.6ns \le t_d \tag{36}$$

$$\le \frac{1}{2 \times 100\text{kHz}} - \frac{1}{2 \times 120\text{kHz}} = 833.33ns. \tag{37}$$

Then deadtime is designed to be 300 ns.

V. Control Method

A. Interleaved Control of the OESS

Three modular converters are interleaved in LV-side-parallel and HV-side-series configuration in this paper to achieve a high conversion ratio. Each module is controlled with a fixed quasi-resonant frequency to achieve ZCS. Since the switching frequency is near to the resonant frequency, the input current is the absolute of the sinusoidal resonant current that will cause large current ripples. The current ripple will be as large as 1.57 times of the average current, causing damage to the battery and leading to large dissipation. Some papers have reported the current ripple should be below 10% of the average current.

In order to reduce the current ripples, this paper adopts a three phases interleaved modulation strategy. The driving sequence and the corresponding waveforms are shown in Fig. 8. Driving signals for the three quasi-resonant converters have a phase shift of 120 degrees to each other. Due to the series input configuration, the total input current is derived as

$$i_i = n i_{peak} \left(|\sin\omega t| + |\sin(\omega t - 2\pi/3)| + |\sin\omega t + 2\pi/3|\right)$$

$$= n i_{peak} \frac{6}{\pi} \left\{ \frac{1}{2} + \sum_{n=1}^{\infty} \left[\frac{1}{6n+1} \sin\left(n + \frac{1}{6}\right)\pi + \frac{1}{6n-1} \sin\left(n - \frac{1}{6}\right)\pi \right] \cos 6n\omega t \right\}. \tag{38}$$

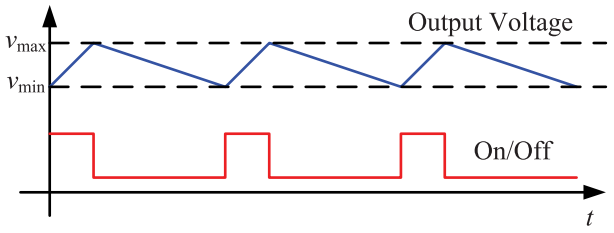

Fig. 9. Driving sequence for output regulation in each modular converter.

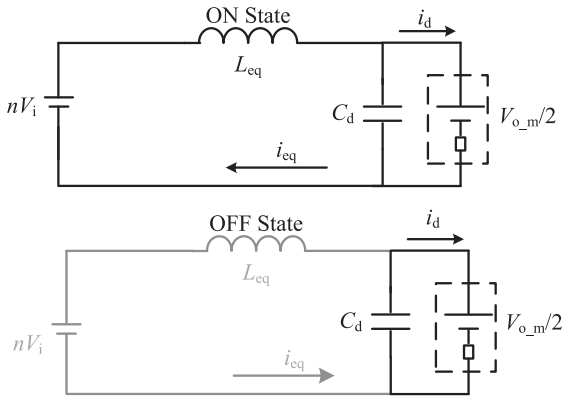

Fig. 10. Equivalent circuit of the proposed converter with burst control method.

The maximum input current ripple is only $\pm 7.0\%$ in theory. The current ripple is significantly reduced by using the interleaved modulation strategy.

B. Burst Control of the Modular Converter

As discussed in Section IV-A, the quasi-resonant frequency can be fixed. In order to achieve output regulation, burst control is used in each modular converter. The driving sequence is shown in Fig. 9. When the output voltage is lower than the minimum value, the quasi-resonant converter is enabled and operates at the quasi-resonant frequency, and the output voltage will rise up. When the output voltage is higher than the maximum value, the quasi-resonant converter will stop working and thus the output voltage will low down. The hysteresis band between the maximum and minimum values decides the output voltage ripple, and the heavy load can result in a higher burst frequency.

In most applications, the burst frequency is far smaller than the switching frequency due to the large output capacitor. Thus, the quasi-resonant converter can be simplified as a logic-controlled voltage source with an equivalent inductor, an output capacitor, and a load resistor as shown in Fig. 10. i_{eq} is the average value of rectifier current and L_{eq} is the equivalent output inductances.

$$i_{eq} = \frac{2}{\pi} |i_{sr}|, \text{and} \tag{39}$$

$$L_{eq} = L_r \frac{\pi^2}{8}. \tag{40}$$

When the switches are enabled, the battery voltage will charge the HV DC bus through the transformer and resonant tank. Similarly, the HV bus capacitor will discharge the HV bus

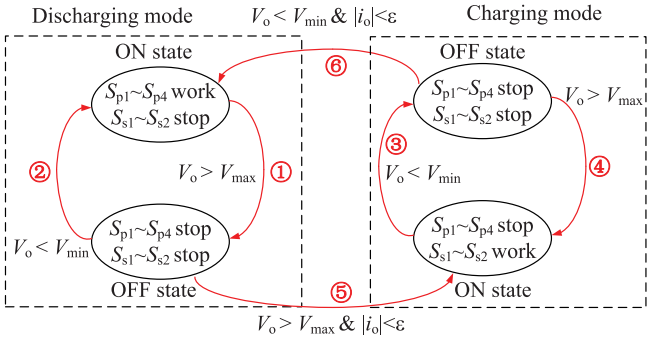

Fig. 11. Control state flow diagram of OESS.

load when the converter is OFF. Define the on-time is T_{on} and off-time is T_{off}. In on-state, the state equations can be derived as

$$L_{eq} \frac{\mathrm{d}i_{eq}}{\mathrm{d}t} = nV_i - V_{o\_m}/2,$$
$$C_d \frac{\mathrm{d}V_{o\_m}}{2\mathrm{d}t} = i_{eq} - i_d. \tag{41}$$

In off-state, the state equations are derived as

$$i_{eq} = 0,$$
$$C_d \frac{\mathrm{d}V_{o\_m}}{2\mathrm{d}t} = i_d. \tag{42}$$

The relationship between voltages and currents of the LV and HV sides can be derived for the voltage variation values of rising and falling are identical.

$$i_d = i_{eq} \frac{T_{on}}{T_{on} + T_{off}}. \tag{43}$$

As shown in (43), i_d can be controlled by regulating the ON- and OFF-time.

When the switches are disabled, the resonant current will cause a large voltage and current spike on the switches. In order to reduce the effect of the resonant energy, all the switches should be turned ON or OFF at the beginning of every switching period. Thus, the resonant current is near to zero at the turn-off time and the EMI is reduced.

C. State Control

The bidirectional DC/DC converter should both charging and discharging operate. Then, the state control between different operating modes is depicted in Fig. 11.

For the discharging mode, during the ON time, the primary switches $S_{p1} - S_{p4}$ are enabled, while the secondary switches $S_{s1} - S_{s2}$ stop working. The output voltage V_o will increase. When $V_o > V_{\max}$, the converter jumps to burst OFF mode via path ①, all switches, i.e., $S_{p1} - S_{p4}$ and $S_{s1} - S_{s2}$, stop working, output voltage V_o will decrease. On the contrary, when $V_o < V_{\min}$, the converter jumps back to burst ON mode via path ②, $S_{p1} - S_{p4}$ are enabled.

For the charging mode, all secondary switches $S_{s1} - S_{s2}$ work to delivering power in a reverse direction to that of the

discharging mode. During burst ON period, $S_{s1} - S_{s2}$ are enabled while $S_{p1} - S_{p4}$ stop working, the output voltage V_o will decrease. When $V_o < V_{\min}$, the converter jumps to burst OFF mode via path ③, all switches, i.e., $S_{p1} - S_{p4}$ and $S_{s1} - S_{s2}$, stop working. The output voltage V_o will increase. When $V_o > V_{\max}$, the converter jumps back to burst ON mode via path ④. $S_{s1} - S_{s2}$ start working again and V_o decreases.

The transition between the discharging mode and the charging mode is determined by V_o and i_o. During burst-OFF time in the discharging mode, when $V_o > V_{max}$ and $\mid i_o \mid < \epsilon$, the converter jumps to burst-on state in charging mode via path ⑤. ϵ represents a minimum value near to zero (for example, 0.01 A). Similarly, during the burst-off period in the charging mode, if $V_o < V_{min}$ and $\mid i_o \mid < \epsilon$, the converter jumps to burst-on state in discharging mode via path ⑥.

Therefore, the output voltage is decided by the control method of OESS.

VI. Discussion

A. Efficiency Merit of ZCS ON and OFF

For the conventional resonant converters with large characteristic impedance in the literature, ZVS ON is commonly used in the MOSFET switches with small turning-off losses, because the junction capacitors of the MOSFET switches can be quickly discharged with a small resonant current through the large resonant inductor quickly. However, if the characteristic impedance is small, the energy that the small resonant inductor can store is not sufficient to discharge the junction capacitors quickly and maintain reverse current going through the MOSFET switches, unless the resonant current becomes sufficiently large. In this case, the instantaneous resonant current at the turn-off time will be very large, resulting in large turn-off losses.

On the contrary, due to the small characteristic impedance, the energy stored in the small resonant inductance can be quickly released during the deadtime, and thus it is motivated to implement both ZCS ON/OFF in the proposed resonant converters for high power efficiency, rather than sole ZVS ON adopted in the conventional resonant converters.

To support the statement above, a numerical comparison is made between the sole ZVS-ON and ZCS ON/OFF modulations in the following.

Conventional sole ZVS ON modulation : Fig. 12 depicts the typical operating waveforms when the power is delivered from the HV side to the LV side. The switching loss for ZVS ON modulation is mainly donated by the turning-off process. The dead time is from t_0 to t_1. During the dead time, both S_{s1} and S_{s2} are OFF, and i_{sr} charges the junction capacitance of the switches. The state equations can be derived as

$$i_{sr} = i_0 \cos\omega_1 t - \frac{nV_i + v_{cr0} + v_{csj0}}{Z_{r1}} \sin\omega_1 t, \tag{44}$$

$$v_{cr} = k_1[Z_{r1} i_0 \sin\omega_1 t + \left(nV_i + \frac{v_{cr0}}{k_1}\right)\cos\omega_1 t] - k_1 n V_i, \tag{45}$$

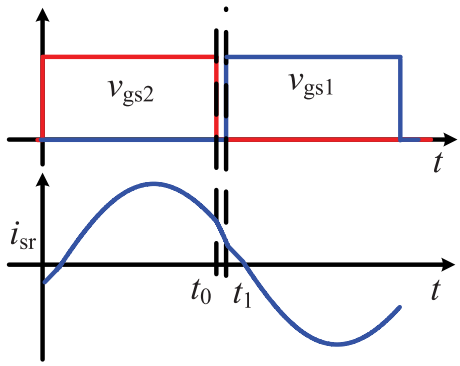

Fig. 12. Operating waveforms of the conventional sole ZVS modulation.

$$v_{csj} = k_2[Z_{r1} i_0 \sin\omega_1 t + (nV_i + \frac{v_{sj0}}{k_2})\cos\omega_1 t] - k_2 n V_i, \tag{46}$$

$$\omega_1 = 2\pi f_{rs}, Z_{r1} = \sqrt{\frac{L_r}{C_{r1}}}, \tag{47}$$

$$k_1 = \frac{C_{sj}}{C_r + C_{sj}}, k_2 = \frac{C_r}{C_r + C_{sj}}. \tag{48}$$

i_0 is the turning-off current at t_0. v_{cr0} and v_{sj0} are the initial voltage values of C_r and C_{sj} at t_0. Since S_{s2} are turned OFF at t_0, v_{sj0} should be equal to the input voltage V_{o_m}.

Please notice that $t_0 - t_1$ is the dead time. The state equations (44) – (48) have small influence on the RMS value of i_{sr} due to the small dead time. And the RMS value of i_{sr} could be indepedent of Z_r when switching frequency is close to resonant one.

The resonant current i_{sr} should be positive to realize ZVS, then the boundary conditions are given by

$$i_0 \cos\omega_1 t_1 - \frac{nV_i + v_{cr0} + v_{csj0}}{Z_{r1}} \sin\omega_1 t_1 \geq 0. \tag{49}$$

By solving (44) to (49), minimum turning-off current i_0 can be achieved for the calculation of switching loss as

$$P_{\text{sw.,ZVS}} = \frac{1}{2} V_{o\_m} i_0 t_{\text{off}} f_s, \tag{50}$$

where t_{off} is the turning-off time.

Proposed ZCS ON/OFF modulation : the operating waveforms have been shown in Fig. 5. The switching loss is mainly donated by the turning-on process and can be calculated by

$$P_{\text{sw.,ZCS}} = \frac{1}{2} C_{sj} V_{o\_m}^2 f_s. \tag{51}$$

Fig. 13 shows the comparison of the switching losses between the proposed ZCS ON/OFF and the conventional sole ZVS ON modulations. It can be observed that the proposed ZCS ON/OFF has efficiency advantages over conventional sole ZVS ON in the proposed small-characteristic-impedance resonant converter, especially in heavy load conditions.

B. Characteristic-Impedance-Independent Magnetic Design

In this paper, a small characteristic impedance Z_r is used for the resonant converter, which could lead to a small resonant

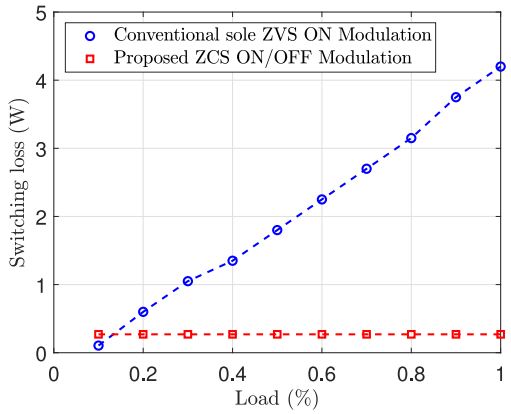

Fig. 13. Switching loss comparison between the ZCS ON/OFF modulation and the conventional sole ZVS ON modulation.

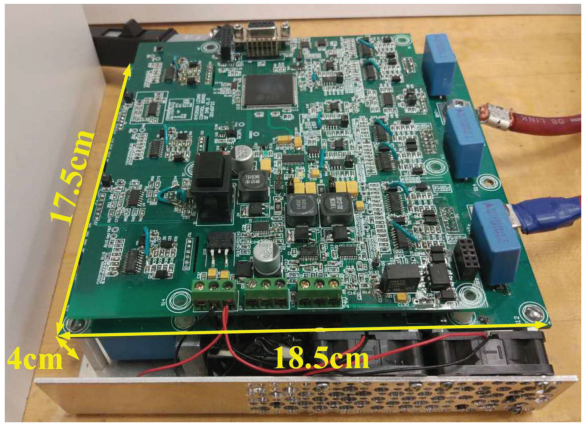

Fig. 14. Prototype of the 5 kW OESS.

inductance achieving high power density. However, the resonant inductor volume and weight are not only up to the values but also up to the resonant current, which are related to its energy, $\frac{1}{2}L_r I_{r\_RMS}^2$.

Other than the traditional method, where the RMS value of i_{sr} is negatively correlated to the characteristic impedance Z_r, the RMS value I_{r_RMS} is only load-related and Z_r-independent in the proposed method. The proof is given as follows.

Since the switching frequency is fixed near to the resonant frequency, the resonant current i_{sr} is approximately sinusoidal and synchronizes with the voltage v_{cd}. The output current I_o can be derived as

$$I_o = \frac{2}{T_s}\int_0^{T_s/2} i_{sr}(t)dt = \frac{2}{\pi}I_{\text{peak}}, \tag{52}$$

where I_{peak} is the amplitude of i_{sr}. I_{r_RMS} is the RMS value of i_{sr} and given by

$$I_{r\_RMS} = \sqrt{\frac{2}{T_s}\int_0^{T_s/2} i_{sr}^2(t)dt} = \frac{I_{\text{peak}}}{\sqrt{2}} = \frac{\pi}{2\sqrt{2}}\frac{V_o}{R}. \tag{53}$$

Therefore, the RMS value I_{r_RMS} is only load-related and Z_r-independent. Such that, we can conclude that the smaller resonant inductor could lead to a smaller volume, achieving high power density.

VII. Experimental Verification

A 5 kW prototype of the proposed OESS is built, as shown in Fig. 14. The OESS interfaces between a 48 V 60 V / 100 A battery source and a 1000 V 1200 V grid bus. The circuit parameters are listed in Table II.

The natural resonant frequency is 120 kHz and the resonant period is 8.33 μs. The reverse recovery charge of the anti-parallel diode of the secondary MOSFET is 0.91 nC. The resonant period of the junction capacitor and resonant capacitor is about 1.2 μs. Therefore, the switching period should be larger than 9.53 μs. The switching frequency is chosen to be 100 kHz with the switching period of 10 μs. The dead time should be larger than 236 ns but smaller than 833 ns. In this paper, the deadtime is designed as 300 ns. With the above settings, all the switches can realize ZCS.

TABLE II
System Parameters

Parameters	Symbols	Values
Rated power	P_N	5 kW
Input voltage	v_i	48 V ~ 60 V
Output voltage	v_o	1000 V ~ 1200 V
Transformer turn ratio	n	3.75
Magnetizing inductance	L_m	1 mH
Leakage inductor	L_r	8 μH
Resonant capacitance	C_r	0.22 μF
Output capacitance	C_1, C_2	4.7 μF
Switching frequency	f_s	100 kHz
Primary switches	S_{p1}–S_{p4}	IRFP4568PBF
Secondary switches	S_{s1}, S_{s2}	FCH104N60F

The size of the proposed 5 kW/100 kHz prototype is only 18.5 cm × 17.5 cm × 4 cm as shown in Fig. 14, achieving a high power density of 3.86 W/cm^3.

A. Steady-State Waveforms

Fig. 15(a) and Fig. 15(b) show the steady-state operating waveforms at 20% and 100% of the rated load, respectively, when the power is delivered from the LV bus side to the HV bus side (discharging mode). The LV bus is 50 V, while the HV bus is 1125 V. The output voltage of each modular converter is 375 V. As shown in the figures, the resonant current reaches zero before the switches are turned OFF, achieving ZCS. When the switches are turned ON, the resonant current is very small, which means the turn-on power loss will be very small. Moreover, the secondary switches can also realize ZCS, no large reverse recovery current occurs.

Fig. 16(a) and Fig. 16(b) show the steady-state operating waveforms at 20% and 90% of the rated load, respectively, when the power is delivered from the HV bus side to the LV bus side (charging mode). Similarly, the secondary and primary switches can also realize ZCS. Since the junction capacitors at the primary side switchers are far smaller than the secondary side, the recovery current in the charging mode is smaller than

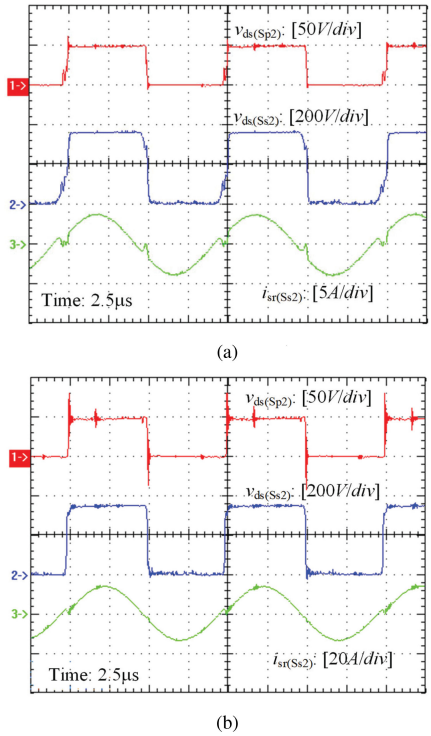

Fig. 15. Measured steady-state operating waveforms of modular converter A in discharging mode when $V_i = 50$ V and $V_{o\_m} = 375$ V.

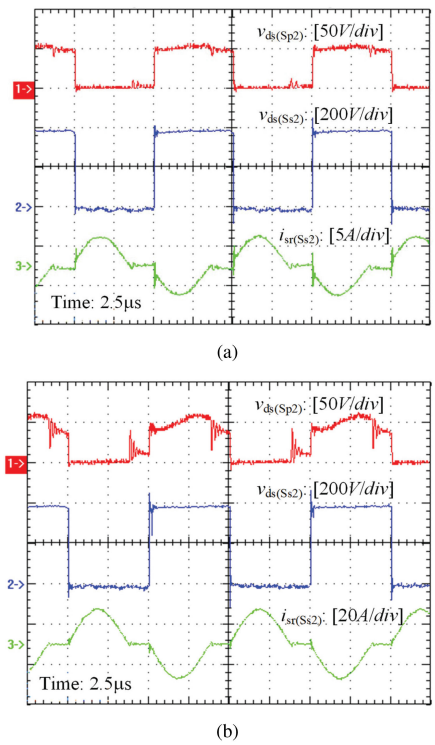

Fig. 16. Measured steady-state operating waveforms of modular converter A in charging mode when $V_i = 50$ V and $V_{o\_m} = 375$ V.

that in the discharging mode. *Mode 2* almost disappears and i_{sr} is zero during *Mode 3* period.

Since the switching frequency is fixed, the variation of load condition just affects the amplitude of the resonant current,

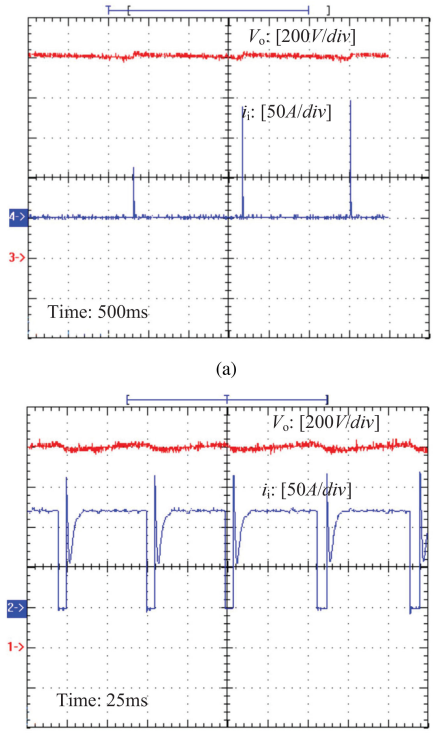

Fig. 17. Measured waveforms of the output voltage and the input current of the OESS under different load conditions.

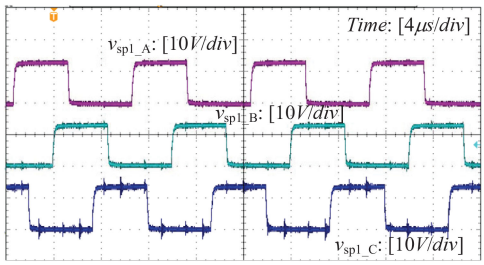

Fig. 18. Measured driving sequence for the three modular quasi-resonant converters.

and soft switching can be achieved at both light and full load conditions, which is consistent with the analysis in Section III.

B. Control and Transient Waveforms

Fig. 17(a) and Fig. 17(b) show the driving sequences and corresponding output waveforms at 20% and 100% of the rated load, respectively. At the light load condition, the converter works for a short interval of time to maintain the output voltage. The burst period is about 1.3 s and the HV bus voltage ripple is about 20 V. At the full load condition, the burst period is about 55 ms.

Fig. 18 shows the interleaved gating signals for the three modular converters to achieve a low current ripple. The gating signals have a phase shift of 120 degrees to each other.

Fig. 19 gives the ripples of input and output current. The green and blue curves are input and output current waveforms

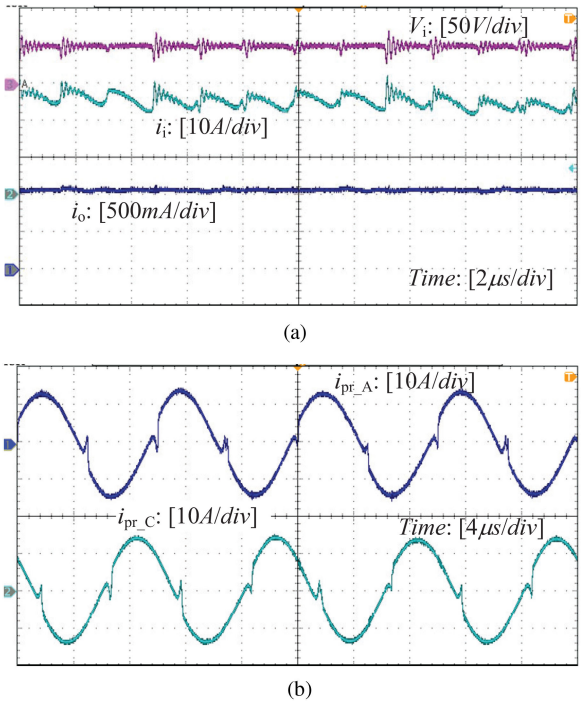

Fig. 19. Measured waveforms of modular current and voltage.

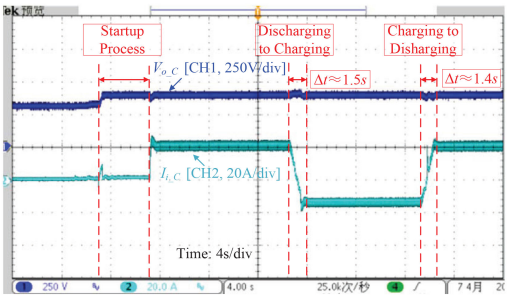

Fig. 20. Transient waveforms of output voltage V_{o_C} and input current I_{i_C} of *Module C* quasi-resonant converter during the transition periods between charging and discharging.

respectively. The input current ripple is as small as ± 2.5 A with a frequency of 600 kHz, corresponding to the analysis. The output current ripple is only about 50 mA. Besides, the phase shift between the resonant current of modules A and C is 120 degrees, which is consistent with the analysis.

Fig. 20 shows the transient waveforms of the output voltage V_{o_C} and the input current I_{i_C} of *Module C* quasi-resonant converter during the transition periods between charging and discharging modes. The scheduling time for charging and discharging is set at around 1.5 s. It can be observed that the transitions are seamless.

C. Efficiency

With the loss analysis with detailed formula derivation process given in the Appendix, the calculated efficiency curves versus the output power are plotted by dashed curves in Fig. 21. Moreover, the measured efficiency curves are plotted by solid curves. It

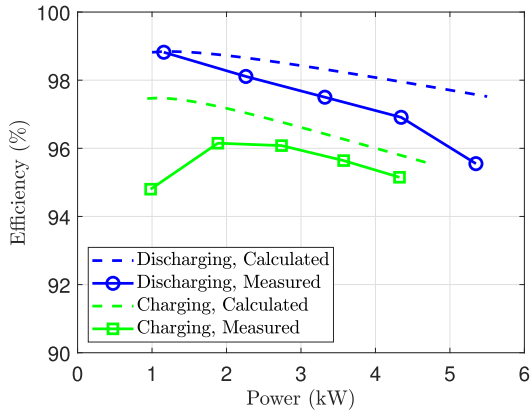

Fig. 21. Efficiency curves of proposed converter at discharging and charging modes.

can be observed that the measured efficiency of the converter is 98.91% at 20% of the rated load and 95.55% at the full load in the discharging mode. When operating in the charging mode, the measured efficiency is 96.15% at 40% of the rated load and 95.15% at the full load. High efficiency can be achieved over the whole load range for the charging and discharging modes.

VIII. Conclusion

A high-conversion-ratio onboard energy storage system is proposed in this paper, which is based on modular-designed quasi-resonant converters with a small characteristic impedance. The modular quasi-resonant converters are in LV-side-parallel and HV-side-series configuration to interface between a HV bus on the grid side and a LV bus on the vehicle side. As the HV bus is up to 1200 V and the LV bus is as low as 48 V, the conversion ratio as high as 20 : 1 for the fast energy exchange. The modular quasi-resonant converters are designed with a small characteristic impedance for the benefits of small volume, low cost, and simple customization, and meanwhile, they can be modulated in a quasi-resonant operation to achieve zero-current-switching ON and OFF for high efficiency. Burst control for output regulation is implemented in each modular converter, while interleaved control is implemented between them to minimize the current ripple. A compact 5 kW experimental prototype achieves a charging/discharging current of 100 A, high efficiency of 98.91%, and a high power density of 3.86 W/cm^3.

APPENDIX

Switching losses: Since ZCS ON/OFF modulation is implemented, the switching losses are caused by the charging and discharging of the parasitic output capacitor of the MOSFET switches and thus can be calculated by

$$P_{\text{switching}} = \frac{1}{2} C_{dc} V_{dc}^2 f \times 4 = 2 C_{dc} V_{dc}^2 f \qquad (54)$$

where C_{ds} is the output capacitance of MOSFETs, V_{dc} is the DC link voltage and f is the switching frequency.

TABLE III
PARAMETERS FOR LOSS CALCULATION

Parameters	Symbols	Values
Output capacitance of switches	C_{ds}	774 pF
On resistance of primary switches	$r_{\text{on,pri.}}$	4.8 m Ω
On resistance of secondary switches	$r_{\text{on,sec.}}$	98 mΩ
Core losses per unit volume	P_v	120 kW/m^3
Core volume	V	13749 mm^3
AC resistor of winding wires	$r_{\text{ac,tri}}$	10.02 mΩ
ESR of resonant capacitor	ESR	18.9 mΩ

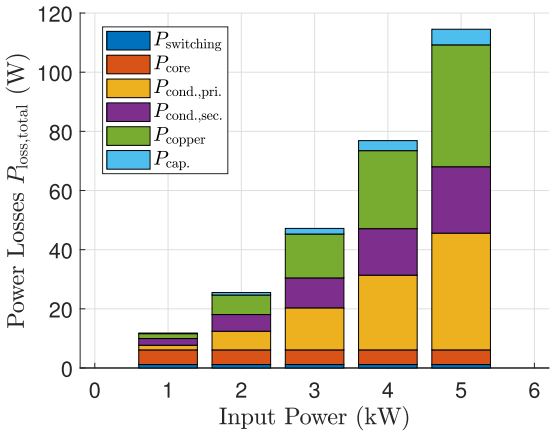

Fig. 22. Power loss ditribution of converter for different input current.

Conduction losses: The primary and secondary conduction losses can be calculated by

$$P_{\text{cond.,pri.}} = 4 \times (\frac{I_{\text{rms,pri.}}}{\sqrt{2}})^2 r_{\text{on,pri.}} = 2I^2_{\text{rms,pri.}} r_{\text{on,pri.}} \quad (55)$$

$$P_{\text{cond.,sec.}} = 2 \times (\frac{I_{\text{rms,sec.}}}{\sqrt{2}})^2 r_{\text{on,sec.}} = I^2_{\text{rms,sec.}} r_{\text{on,sec.}} \quad (56)$$

where $r_{\text{on,pri.}}$ and $r_{\text{on,sec.}}$ are the conducting resistance of the primary and secondary switches respectively. $I_{\text{rms,pri.}}$ and $I_{\text{rms,sec.}}$ are the root mean square values of the resonant current in the primary and secondary sides respectively.

Core losses: In the proposed OESS system, ELP 43/10/28 N97 core is used to construct the transformer. The core losses can be calculated by

$$P_{\text{core}} = P_v V \quad (57)$$

where P_v is the core losses per unit volume that can be looked up in the datasheet according to the frequency, temperature, and magnetic flux density, and V is the volume of the magnetic core.

Copper losses: The copper losses can be calculated by

$$P_{\text{copper}} = I^2_{\text{rms,pri.}} r_{\text{ac,tri}} \quad (58)$$

where $r_{\text{ac,tri.}}$ is the equal AC resistor of transformer winding wires considering the skin effect and the proximity effect caused by the high switching frequency. The AC resistor is about several times of the transformer winding wires DC resistor.

Capacitance losses: The losses of the resonant capacitor caused by the ESR of the capacitors can be calculated by

$$P_{\text{cap.}} = I^2_{\text{rms,sed.}} \text{ESR} \quad (59)$$

The total losses can be calculated by

$$P_{\text{loss,total}} = P_{\text{switching}} + P_{\text{cond.,pri.}} + P_{\text{cond.,sec.}} \quad (60)$$

$$+ P_{\text{core}} + P_{\text{copper}} + P_{\text{cap.}} \quad (61)$$

With detailed parameters for loss calculation given in Table III, Fig. 22 shows the loss distribution.

REFERENCES

[1] A. Emadi, Y. J. Lee, and K. Rajashekara, "Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237–2245, Jun. 2008.
[2] S. Gao, K. T. Chau, C. Liu, D. Wu, and C. C. Chan, "Integrated energy management of plug-in electric vehicles in power grid with renewables," *IEEE Trans. Veh. Tech.*, vol. 63, no. 7, pp. 3019–3027, Sep. 2014.
[3] V. Monteiro, J. G. Pinto, and J. L. Afonso, "Operation modes for the electric vehicle in smart grids and smart homes: Present and proposed modes," *IEEE Trans. Veh. Tech.*, vol. 65, no. 3, pp. 1007–1020, Mar. 2016.
[4] H. Turker and S. Bacha, "Optimal minimization of plug-in electric vehicle charging cost with vehicle-to-home and vehicle-to-grid concepts," *IEEE Trans. Veh. Tech.*, vol. 67, no. 11, pp. 10281–10292, Nov. 2018.
[5] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.
[6] V. Monteiro, J. C. Ferreira, A. A. N. Melendez. C.Couto and J. L.Afonso, "Experimental validation of a novel architecture based on a dual-stage converter for off-board fast battery chargers of electric vehicles," *IEEE Veh. Tech.*, vol. 67, no. 2, pp. 1000–1011, Feb. 2018.
[7] L. Tan, B. Wu, V. Yaramasu, S. Rivera, and X. Guo, "Effective voltage balance control for bipolar-DC-bus-fed EV charging station with three-level DC-DC fast charger," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4031–4041, Jul. 2016.
[8] H. Haga, and F. Kurokawa, "Modulation method of a full-bridge three-level LLC resonant converter for battery charger of electrical vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2498–2507, Apr. 2017.
[9] Z. U. Zahid, Z. M. Dalala, R. Chen, B. Chen, and J. S. Lai, "Design of bidirectional DC/DC resonant converter for vehicle-to-grid (V2G) applications," *IEEE Trans. Transport. Electrific.*, vol. 1, no. 3, pp. 232–244, Oct. 2015.
[10] F. Krismer, and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.
[11] F. Krismer, and J. W. Kolar, "Efficiency-optimized high-current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.
[12] W. Drury, C. Patel, A. Atkins, and A. Wearing, "High power density, 48 V electrified drivetrain technology for future hybrid and electric vehicles," *SAE Int. J. Adv. Curr. Prac. Mobility*, vol. 1, no. 1, pp. 55–60, Jan. 2019.
[13] R. W. DeDoncker, M. H. Kheraluwala, and D. M. Divan, "Power conversion apparatus for DC/DC conversion using dual active bridges," U.S. Patent, 5027264, Jan. 1991.
[14] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.
[15] J. Everts, "Closed-form solution for efficient ZVS modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7561–7576, Oct. 2017.
[16] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional DC/DC converter based on dual-phase-shift control for DC distribution application," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1711–1727, Apr. 2013.
[17] A. K. Jain, and R. Ayyanar, "PWM control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1215–1227, Apr. 2011.
[18] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC-DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237–1248, Mar. 2012.
[19] Y. Lu, W. U. Q., Q. Wang, D. Liu, and L. Xiao, "Analysis of a novel zero-voltage-switching bidirectional DC/DC converter for energy storage system," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3169–3179, Apr. 2017.

[20] G. G. Oggier, G. O. Garcla, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1826–1838, Jul. 2009.
[21] F. Krismer and J. W. Kolar, "Accurate small-signal model for the digital control of an automotive bidirectional dual active bridge," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2756–2768, Dec. 2009.
[22] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Dead-time effect of the high-frequency isolated bidirectional full-bridge DC-DC converter: Comprehensive theoretical analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1667–1680, Apr. 2014.
[23] N. Hou, W. Song, and M. Wu, "Minimum-current-stress scheme of dual active bridge DC-DC converter with unified phase-shift control," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8552–8561, Dec. 2016.
[24] J. Hiltunen, V. Vaisanen, R. Juntunen, and P. Silventoinen, "Variable-frequency phase shift modulation of a dual active bridge converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7138–7148, Dec. 2015.
[25] H. Bai, and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC/DC converters using novel dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.
[26] W. Chen, P. Rong, and Z. Lu, "Snubberless bidirectional DC-DC converter with new CLLC resonant tank featuring minimized switching loss," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3075–3086, Sep. 2010.
[27] J. H. Jung, H. S. Kim, M. H. Ryu, and J. W. Baek, "Design methodology of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems," *IEEE Trans. Power. Electron.*, vol. 28, no. 4, pp. 1741–1755, Apr. 2013.
[28] C. Zhang, P. Li, Z. Kan, X. Chai, and X. Guo, "Integrated half-bridge CLLC bidirectional converter for energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3879–3889, May 2018.
[29] S. Zou, J. Lu, A. Mallik, and A. Khaligh, "Bidirectional CLLC converter with synchronous rectification for plug-in electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 998–1005, Mar. 2018.
[30] B. Li, Q. Li, and F. C. Lee, "High-frequency PCB winding transformer with integrated inductors for a bi-directional resonant converter," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6123–6135, Jul. 2019
[31] P. He, A. Mallik, A. Sankar, and A. Khaligh, "Design of a 1-MHz high-efficiency high-power-density bidirectional GaN-based CLLC converter for electric vehicles," *IEEE Trans. Veh. Tech.*, vol. 68, no. 1, pp. 213–223, Jan. 2019.
[32] C. Bai, B. Han, B. Kwon, and M. Kim, "High efficiency bidirectional series-resonant DC/DC converter over wide range of battery voltage," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3636–3650, Apr. 2020
[33] C. Fei, Y. Yang, Q. Li, and F. C. Lee, "Shielding technique for planar matrix transformers to suppress common-mode EMI noise and improve efficiency," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1263–1272, Feb. 2018.
[34] M. Li, Z. Ouyang, and M. A. E. Andersen, "High frequency LLC resonant converter with magnetic shunt integrated planar transformer," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2405–2415, Mar. 2019.
[35] S. Zou, J. Lu, A. Mallik, and A. Khaligh, "Modeling and optimization of an integrated transformer for electric vehicle on-board charger applications," *IEEE Trans. Transport. Electric.*, vol. 4, no. 2, pp. 355–363, Feb. 2018.
[36] F. Xue, R. Yu,and A. Q. Huang, "A 98.3% efficient GaN isolated bidirectional DC-DC converter for DC microgrid energy storage system applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9094–9103, Nov. 2017.

Zhijian Fang (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering and automation from the Huazhong University of Science and Technology, Wuhan, China, in 2010 and 2015, respectively.

From 2015 to 2018, he was a Postdoctoral Research Fellow with the School of Electrical Engineering, Wuhan University, Wuhan, China. From February 2016 to January 2017, he was a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. Since 2019, he has been a Professor with the School of Automatic, China University of Geosciences, Wuhan, China. His research interests include high performance DC/DC converter, battery charger, and renewable energy applications

Zhiguo Wei received the bachelor's degree in automation from Inner Mongolia University, Hohhot, China, in 2019. He is currently working toward the master's degree in control engineering with the China University of Geosciences, Wuhan, China. His research focuses on power electronic converter and its control.

Zhicong Huang (Member, IEEE) received the B.Eng. degree in electrical engineering and automation and the M.Phil. degree in mechanical and electronic engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2010 and 2013, respectively, and the Ph.D. degree in power electronics from The Hong Kong Polytechnic University, Hong Kong, in 2018.

He is currently an Assistant Professor with the Shien-Ming Wu School of Intelligent Engineering, South China University of Technology, Guangzhou, China. His research interests include wireless power transfer, resonant converter, electric vehicle, and intelligent engineering. He was the recipient of the UM Macao Talent Program in 2018 and Best Track Paper Award by IEEE PES APPEEC in 2019.

Fei Liu (Senior Member, IEEE) was born in Hanchuan, Hubei Province, China, in 1977. He received the B.S., M.S., and Ph.D. degrees from the Huazhong University of Science and Technology, Wuhan, China, in 2000, 2004, and 2008, respectively.

Since 2010, he has been a Faculty Member with Wuhan University, Wuhan, China. He is currently a Professor with the School of Electrical Engineering, Wuhan University. His research interests include DC microgrid and cascaded multilevel converter.